INTEGRATED CIRCUITS

Semiconductors for Radio and Audio Systems

1997

Data Handbook IC01

Let's make things better.

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Radio and Audio Systems

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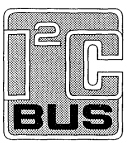
DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

PREFACE

The audio/video market is characterized by a continuing demand for innovation to increase the functionality of ICs by achieving ever higher levels of integration, reducing power consumption, minimizing the number of peripheral components and reducing the need for circuit alignment during assembly. We achieve these goals by extensive use of computer control via the I2C-bus, and by designing analog, digital and mixed signal circuits using the very latest signal processing techniques. We then fabricate the ICs with state-of-the-art production processes so we can offer you complete `systems-on-silicon' which help you maintain your competitive edge by staying one step ahead of the competition.

An innovative and reliable supplier

A total systems approach, embracing both hardware and software, is the foundation on which we have built our unrivalled reputation as an innovative and reliable supplier of high quality semiconductors for the audio/video segments of the consumer electronics market.

Our strengths in this field stem not only from being a large multinational organization with the resources to stay the course, but also from our dedication to research and to forming true and lasting partnerships with our customers.

World-class manufacturing, resources and customer support

Philips Semiconductors is a global supplier. We employ some 20,000 people, have more than 100 sales offices worldwide, are represented in 44 countries, and manufacture over 14,000 different products. Philips also has a level of commitment to research matched by very few companies, not just in terms of resources but in their focus on researching solutions for customers. Philips Semiconductors collaborates very closely with Philips Corporate Research Laboratories, one of the largest privately funded research organisations in the world. Five major research laboratories serve the whole group, in the Netherlands, UK, France, Germany and the USA.

As you would expect from a worldwide organization, our support doesn't end with the timely delivery of ICs and discretes to our audio/video customers. We are also dedicated to the aim of zero-defects quality for our semiconductors, and to offering unequalled service. There are Philips customer support and application centres in every major market area (Europe, Asia-Pacific, North America) to ensure that you can take full advantage of our extensive applications know-how and broad product range. Four Product Concept and Applications Laboratories are involved in programs and activities relevant to audio/video: Eindhoven, the Netherlands (TV, monitors and radio/audio); Hamburg, Germany (TV and radio/audio); Southampton, UK (teletext and digital audio, including CD technology).

They support all audio/video applications and work closely with customers, meeting and often anticipating their needs.

Many key developments have come from Philips laboratories - one-chip TV signal processors, ICs for memory-based TV features, a TV microcontroller with on-chip teletext, a two-chip receiver module for car radio, and a one-chip self-tuned radio are just a few examples. In addition, there are also Product Development groups in all the above locations.

Partnership

Since the spur for many of the ICs and discrete semiconductors in this databook have come from a cross-fertilisation of ideas with customers, we are fully aware that we need to be not only semiconductor suppliers, but also partners who are willing to work with customers to find solutions and help keep them at the leading edge of their field. At Philips Semiconductors, we work very closely with our audio/video customers and are determined to maintain a reputation for being the world's most customer-oriented supplier.

WHAT THIS BOOK AND CD-ROM CONTAIN

This book is a supplement to the existing databook IC01 - Semiconductors for radio and audio, and contains abstracts of our latest datasheets. In addition, all the datasheets found in IC01 and this supplement are contained on the accompanying CD-ROM. The datasheet files on the CD-ROM are in Adobe's Portable Document Format (PDF) - a cross-platform file format that requires Acrobat Reader to view (we have also supplied Acrobat Reader on the CD-ROM). Acrobat Reader enables you to view and print pages, and perform basic searches. Please refer to the READ.ME file on the CD-ROM for information on the CD's contents and organization, as well as instructions how to install and use Acrobat Reader.

FOR MORE INFORMATION

Although the information in this databook is up-to-date at the time of going to press, the world of audio/video is so fast moving it is possible that some very recent developments may not have made it into this edition. For the latest information contact your local Philips organization (see the back page of this databook for addresses), or visit our Internet home page at: http://www.semiconductors.philips.com/ps/

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REPLACED/WITHDRAWN TYPES

The following type numbers were in the previous issue of this data handbook, but not in the current version:

TYPE NUMBER	REPLACED BY	REASON FOR DELETION
P8xC592	-	In IC18
P8xCE598	-	In IC19
PCF2115	-	Discontinued
SAA7322/SAA7323	-	Discontinued
SAA7350	-	Discontinued
SAA7501	-	customized/out
TDA1303T	-	Discontinued
TDA1542	-	Discontinued
TDA1543(A)/S6	-	Discontinued
TDA1543A	-	Discontinued
TDA1544	-	Discontinued
TDA1578A	-	Discontinued
TDA1593_1	-	Discontinued
TDA3047	-	Taken out by on request of HB owner
TDA3048	-	Taken out by on request of HB owner
TEA0657	-	Discontinued
TEA5580	-	Discontinued
TEA5592	-	Discontinued
PCF8568	-	Discontinued
PCF8569		PCF8579

GENERAL

TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A Germanium or other material with a band gap of 0.6 to 1 eV

B Silicon or other material with a band gap of 1 to 1.3 eV

C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A Diode; signal, low power

B Diode; variable capacitance

C Transistor; low power, audio frequency

D Transistor; power, audio frequency

E Diode; tunnel

F Transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under "Serial number/special third letter"

H Diode; magnetic sensitive

L Transistor; power, high frequency

N Photocoupler

P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q Radiation generator; e.g. LED, laser; with special third letter

R Control or switching device; e.g. thyristor, low power; with special third letter

S Transistor; low power, switching

T Control and switching device; e.g. thyristor, power; with special third letter

U Transistor; power, switching

W Surface acoustic wave device

X Diode; multiplier, e.g. varactor, step recovery

Y Diode; rectifying, booster

Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A For triacs, after second letter 'R' or 'T'

F For emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L For lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O For opto-triacs, after second letter 'R'

T For 3-state bicolour LEDs, after second letter 'Q'

W For transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112 Germanium, low power signal diode (consumer type)

ACY32 Germanium, low power AF transistor (industrial type)

BD232 Silicon, power AF transistor (consumer type)

CQY17 GaAs, light-emitting diode (industrial type)

RPY84 CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%

B 2%

C 5%

D 10%

E 20%.

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to + 70 °C

C –55 to +125 °C

D –25 to + 70 °C

E –25 to + 85 °C

F –40 to + 85 °C

G –55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C Cylindrical

D Dual in-line (DIL)

E Power DIL (with external heatsink)

F Flat pack (leads on two sides)

G Flat pack (leads on four sides)

H Quad flat pack (QFP)

K Diamond (TO-3 family)

M Multiple in-line (except dual, triple and quad)

Q Quad in-line (QUIL)

R Power QUIL (with external heatsink)

S Single in-line (SIL)

T Triple in-line

W Leaded chip carrier (LCC)

X Leadless chip carrier (LLCC)

Y Pin grid array (PGA).

SECOND LETTER (MATERIAL)

C Metal-ceramic

G Glass-ceramic

M Metal

P Plastic.

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

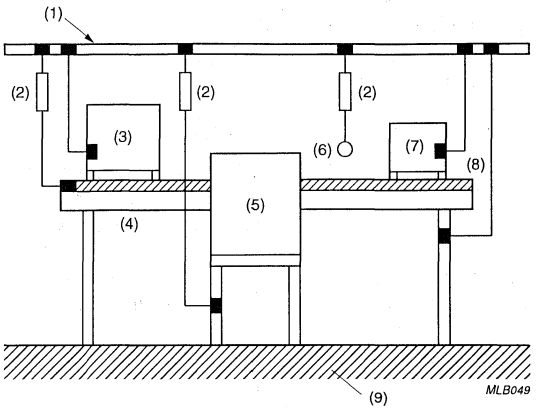
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

FEATURES

- Local/DX switching to improve large signal handling on FM when an outdoor antenna or cable network is connected
- Local/DX function provides different search levels which are useful for spectrum analyser functions
- Three extra I/O expander ports are available for general purpose (I^2C-bus only)
- RDS-MPX signal available
- The module meets the *"FCC regulations"*
- The OM5604; OM5606 is in accordance with *"CENELEC EN55022"* and *"CENELEC EN50082-1"*.

GENERAL DESCRIPTION

The OM5604; OM5606 is an FM-radio tuner which includes a brand new concept in tuning techniques. The new tuning concept combines the advantages of hand tuning together with electronic facilities and features. The tuner is I^2C-bus controlled.

ANTENNA CONNECTOR

RF connector

- OM5604: F-connector (FM input impedance = 75 Ω)
- OM5606: IEC-connector (FM input impedance = 75 Ω).

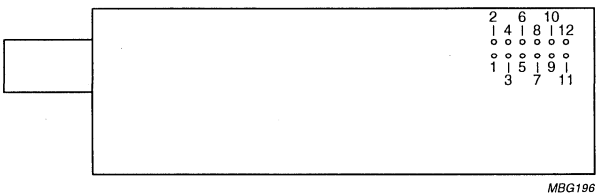


Fig.1 OM5604; OM5606 connector.

ORDERING INFORMATION

UNIT	FREQUENCY (MHz)	BUS	RF CONNECTOR
FM I^2C-bus	87.5 to 108	I^2C-bus	F-connector for OM5604
			IEC-connector for OM5606

PINNING

PIN	DESCRIPTION
1	port 5 PCF8574A (I^2C-bus)
2	port 6 PCF8574A (I^2C-bus)
3	port 7 PCF8574A (I^2C-bus)
4	serial clock input[1]
5	stereo indicator
6	serial data input/output[1]
7	supply voltage (+5 V)
8	supply voltage (+12 V)
9	audio right output
10	ground
11	audio left output
12	MPX signal for RDS demodulation

Note

1. See *"The I^2C-bus and how to use it"* (ordering number 9398 393 40011).

INTERFACE

- Digital driving: I^2C-bus
- Audio output: typical 900 mV RMS (load 600 Ω) for FM Δf = 75 kHz
- Supply: 5 V ±10% current ≤30 mA and 12 V ±1%, ripple ≤1 V, current ≤2 mA
- RDS-MPX: DC coupled (load ≥39 kΩ), amplitude typical 150 mV (Δf = 75 kHz)
- RF input connector (75 Ω)
- 12 pin connector.

LIMITING VALUES

IEC publication 68-1; full specification; EMC behaviour: the module is designed to be FCC friendly (part 15).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T	temperature		15	35	°C
RH	relative humidity		25	85	%
T_{amb}	operating ambient temperature	functional operation	–10	+60	°C
T_{stg}	storage temperature		–20	+70	°C
$V_{esd(pc)}$	electrostatic handling for pin connector	note 1	–	2	kV
		note 2	–	300	V
$V_{esd(RFc)}$	electrostatic handling for RF-connector	note 3	–	4	kV
		note 4	–	500	V

Notes

1. Class B: human body model (1.5 kΩ, 100 pF).
2. Class B: charge device model (0 Ω, 200 pF).
3. Class A: human body model (1.5 kΩ, 100 pF).
4. Class A: charge device model (0 Ω, 200 pF).

FEATURES

- Local/DX switching to improve large signal handling on FM when an outdoor antenna or cable network is connected
- Local/DX function provides different search levels which are useful for spectrum analyser functions
- Three extra I/O expander ports are available for general purpose (I²C-bus only)
- MPX signal available
- The module meets the *"FCC regulations"*
- The OM5608 operates in accordance with *"CENELEC EN55022"* and *"CENELEC EN50082-1"*.

GENERAL DESCRIPTION

The OM5608 is an FM-radio tuner which includes a brand new concept in tuning techniques. The new tuning concept combines the advantages of hand tuning together with electronic facilities and features. The tuner is I²C-bus controlled and designed for the Japanese FM-band.

ANTENNA CONNECTOR

RF connector

- RF-connection: F-connector (FM input impedance = 75 Ω).

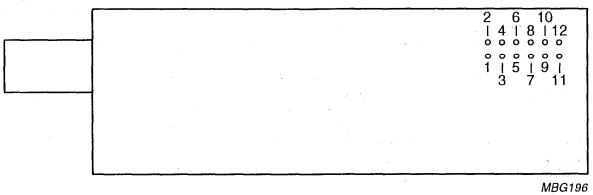


Fig.1 F-connector.

ORDERING INFORMATION

UNIT	FREQUENCY (MHz)	BUS	RF CONNECTOR
FM I²C-bus	76 to 90	I²C-bus	F-connector

PINNING

PIN	DESCRIPTION
1	port 5 PCF8574A (I^2C-bus)
2	port 6 PCF8574A (I^2C-bus)
3	port 7 PCF8574A (I^2C-bus)
4	SCL; serial clock input[1]
5	stereo indicator
6	SDA; serial data input/output[1]
7	supply voltage (+5 V)
8	supply voltage (+12 V)
9	audio right output
10	ground
11	audio left output
12	MPX signal

Note

1. See *"The I^2C-bus and how to use it"* (ordering number 9398 393 40011).

INTERFACE

- Digital driving: I^2C-bus
- Audio output: typical 900 mV RMS (load 600 Ω) for FM Δf = 75 kHz
- Supply:

  5 V ±10% current ≤30 mA and

  12 V ±1%, ripple ≤1 V, current ≤2 mA
- MPX: DC coupled (load ≥39 kΩ), amplitude typical 150 mV (Δf = 75 kHz)
- RF input connector (75 Ω)
- 12 pin connector.

LIMITING VALUES

IEC publication 68-1; full specification; EMC behaviour: the module is designed to be FCC friendly (part 15).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T	temperature		15	35	°C
RH	relative humidity		25	85	%
T_{amb}	operating ambient temperature	functional operation	–10	+60	°C
T_{stg}	storage temperature		–20	+70	°C
$V_{esd(pc)}$	electrostatic handling for pin connector	note 1	–	2	kV
		note 2	–	300	V
$V_{esd(RFc)}$	electrostatic handling for RF-connector	note 3	–	4	kV
		note 4	–	500	V

Notes

1. Class B: human body model (1.5 kΩ, 100 pF).
2. Class B: charge device model (0 Ω, 200 pF).
3. Class A: human body model (1.5 kΩ, 100 pF).
4. Class A: charge device model (0 Ω, 200 pF).

Digital Servo Driver (DSD-2) OQ8844

FEATURES

Servo functions

- 1-bit class-D focus actuator driver (3.3 Ω)
- 1-bit class-D radial actuator driver (3.7 Ω)
- 1-bit class-D sledge motor driver (2.5 Ω).

Other features

- Supply voltage 5 V only
- Small package (SOT163-1)
- Higher efficiency, compared with conventional drivers, due to the class-D principle
- Built-in digital notch filters for higher efficiency
- Enable input for focus and radial driver
- Enable input for sledge driver
- Differential outputs for all drivers
- Separate power supply pins for all drivers.

GENERAL DESCRIPTION

The OQ8844 or Digital Servo Driver 2 (DSD2) consists of 1-bit class-D power drivers, which are specially designed for digital servo applications. Three such amplifiers are integrated in one chip, to drive the focus and radial actuators and the sledge motor of a compact disc optical system.

The main benefits of using this principle are its higher efficiency grade compared to conventional analog power amplifiers, its higher integration level, its differential output and the fact that only a few external components are needed. When using these digital power drivers in a digital servo application, the statement 'complete digital servo loop' becomes more realistic.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	4.5	–	5.5	V
$V_{DD(F)}$	supply voltage focus actuator	4.5	–	5.5	V
$V_{DD(R)}$	supply voltage radial actuator	4.5	–	5.5	V
$V_{DD(S)}$	supply voltage sledge actuator	4.5	–	5.5	V
I_{DDDq}	quiescent supply current digital part	–	–	10	μA
$I_{DD(F)}$	supply current focus	–	126	250	mA
$I_{DD(R)}$	supply current radial	–	20	250	mA
$I_{DD(S)}$	supply current sledge	–	150	560	mA
$f_{i(clk)}$	input clock frequency	–	4.2336	5	MHz
P_{tot}	total power dissipation	–	110	–	mW
T_{amb}	operating ambient temperature	−40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ8844	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

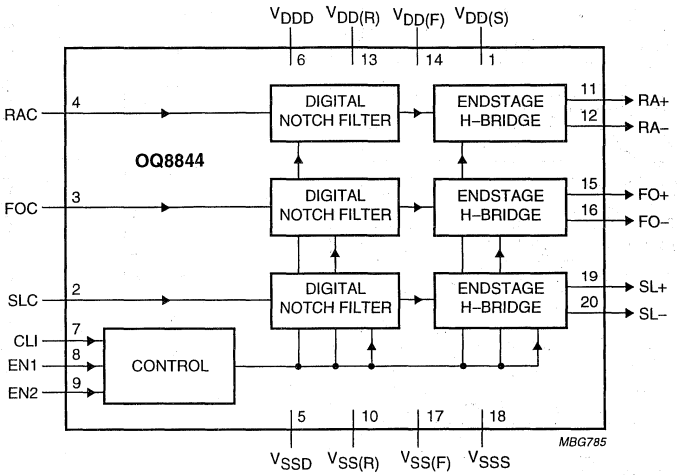


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{DD(S)}$	1	supply voltage for sledge motor driver
SLC	2	PDM input for sledge driver
FOC	3	PDM input for focus driver
RAC	4	PDM input for radial driver
V_{SSD}	5	digital ground
V_{DDD}	6	digital supply voltage
CLI	7	clock input
EN1	8	enable input 1
EN2	9	enable input 2
$V_{SS(R)}$	10	radial driver ground
RA+	11	radial driver (positive output)
RA–	12	radial driver (negative output)
$V_{DD(R)}$	13	radial supply voltage
$V_{DD(F)}$	14	focus supply voltage
FO+	15	focus driver (positive output)
FO–	16	focus driver (negative output)
$V_{SS(F)}$	17	focus ground
V_{SSS}	18	sledge driver ground
SL+	19	sledge driver (positive output)
SL–	20	sledge driver (negative output)

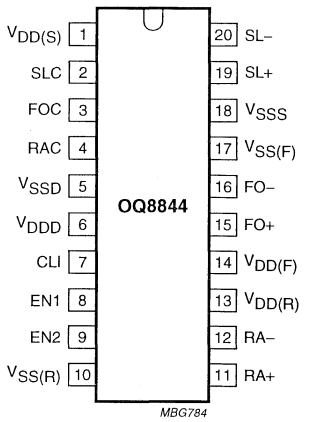
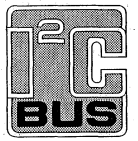


Fig.2 Pin configuration.

Digital Servo Integrated Circuit Silent (DSICS)

OQ8868

FEATURES



The DSICS realizes the following servo functions:

- Focus servo loop
- Radial servo loop
- Built-in access procedure
- Sledge motor servo loop
- Three line (TDA1301T-like; same on hardware level, coefficients differ) or I²C-bus serial interface with system controller.

Other features are:

- Single supply voltage (5 V)
- Flexible system oscillator
- Usable for single/double Foucault and astigmatic focus
- Wide range of adjustable servo characteristics possible
- Automatic focus start-up procedure and in-lock indication
- Fast focus restart procedure
- Sophisticated track loss detection mechanism
- Extended radial error signal
- Automatic initialization and jump procedure for radial servo
- Automatic radial error gain and offset control
- Sophisticated defect detector
- Shock detector
- Fast serial communication
- Low noise servo loops
- Automatic gain control for the complete focus and radial loop
- Fast track counting signal input
- Steered sledge jump
- Radial actuator damping.

Features that improve on its predecessor, the TDA1301T:

- Low noise in the focus loop
- Faster serial communication
- Improved jump performance.

Added features are:

- High level watchdogs
- Decoder (LO9585, LO9588 or HD60) communication support
- Application debugging support
- Pulsed sledge mode
- Auto gain control on radial and focus loop
- I²C-bus serial communication
- Externally available defect detector signals.

GENERAL DESCRIPTION

The Digital Servo Integrated Circuit Silent (DSICS) IC provides all servo functions except the spindle motor control in two-stage Compact Disc (CD) systems. It offers a high degree of integration, combined with the low additional cost of external components. The servo characteristics are widely adjustable by means of a three-wire serial interface, which offers great flexibility for the application of different CD mechanisms.

The servo chip accepts diode currents and drives various power stages. Proper functioning of the focus and radial AGCs requires a digital power stage (OQ8844 or SZA1010). It can drive normal, CDM12-like, mechanisms.

It is the improved version of its predecessor, the DSIC2 (TDA1301).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ8868	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	–	5.5	V
V_{DDA}	analog supply voltage		4.5	–	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
$I_{DD(q)}$	digital quiescent supply current		–	–	10	µA
I_{DDA}	analog supply current		–	5	–	mA
I_I	input current					
	for pins D1 to D4	note 1	–	–	12	µA
	for pins S1 and S2	note 2	–	–	6	µA
P_{tot}	total power dissipation		–	115	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

Notes

1. Maximum input range varies from 3.8 to 12 µA and varies with the reference current through XTLR.
2. Maximum input range varies from 1.9 to 6 µA and varies with the reference current through XTLR.

BLOCK DIAGRAM

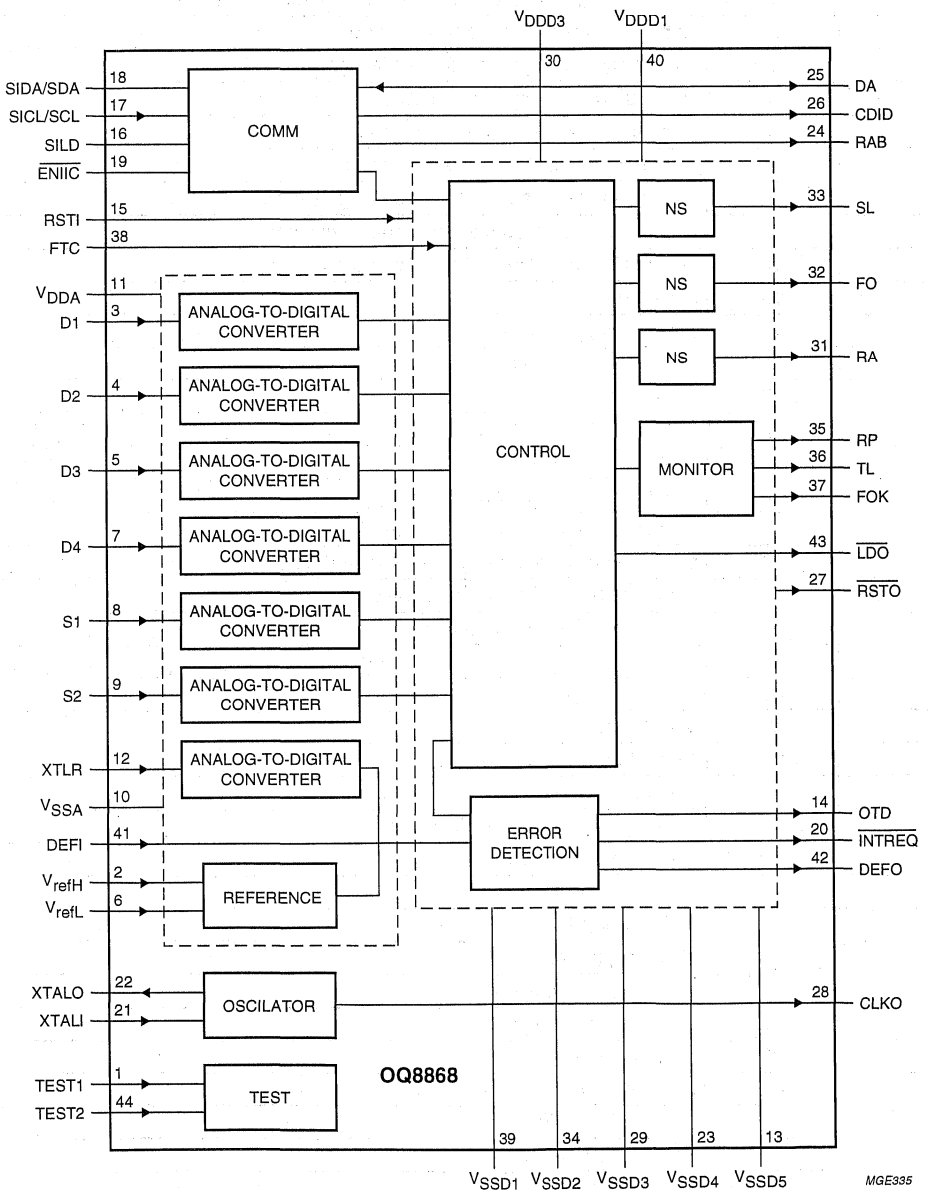


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TEST1	1	test input 1 (LOW for normal operation); internal pull-down
V_{refH}	2	high reference for A/D converter (input)
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{refL}	6	low reference for A/D converter (input)
D4	7	unipolar current input (central diode signal input)
S1	8	unipolar current input (central diode signal input)
S2	9	unipolar current input (central diode signal input)
V_{SSA}	10	analog ground
V_{DDA}	11	analog supply voltage
XTLR	12	reference current input
V_{SSD5}	13	digital ground 5
OTD	14	off track detector (output)
RSTI	15	reset input (active HIGH)
SILD	16	serial host interface load
SICL/SCL	17	serial host interface clock /I²C-bus clock (SCL)
SIDA/SDA	18	serial host interface data /I²C-bus data (SDA)
$\overline{\text{ENIIC}}$	19	enable I²C-bus serial format (active LOW)
$\overline{\text{INTREQ}}$	20	interrupt request output (active LOW)
XTALI	21	oscillator input
XTALO	22	oscillator output
V_{SSD4}	23	digital ground 4
RAB	24	serial decoder interface load (output)
DA	25	serial decoder interface data (input/output)
CDIC	26	serial decoder interface clock (output)
$\overline{\text{RSTO}}$	27	reset output (active LOW)
CLKO	28	clock buffer output
V_{SSD3}	29	digital ground 3
V_{DDD3}	30	digital supply voltage 3
RA	31	radial actuator output
FO	32	focus actuator output
SL	33	sledge output
V_{SSD2}	34	digital ground 2
RP	35	radial polarity signal
TL	36	track loss signal
FOK	37	focus OK output
FTC	38	fast track counting input (internal pull-down)
V_{SSD1}	39	digital ground
V_{DDD1}	40	digital supply voltage 1

SYMBOL	PIN	DESCRIPTION
DEFI	41	defect detector input (connected to DEFO)
DEFO	42	defect detector output
$\overline{LDO}$	43	laser drive on output (open drain, active LOW)
TEST2	44	test input 2 (low for normal operation)

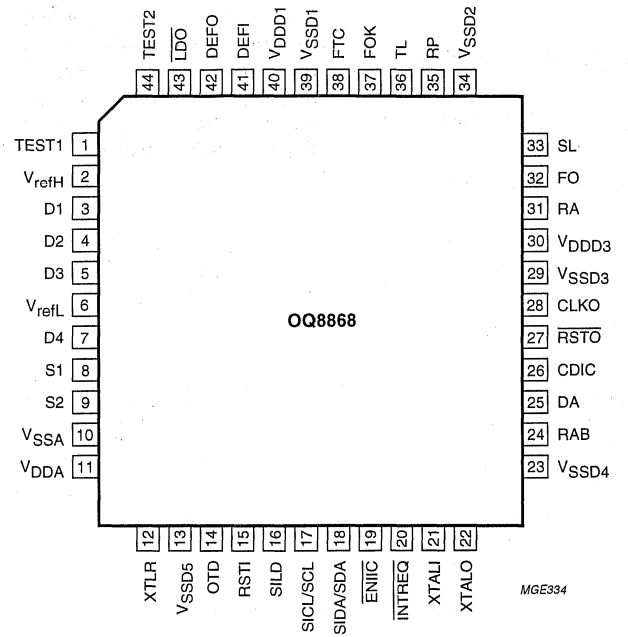


Fig.2 Pin configuration.

Stereo filter and codec SAA2003

FEATURES

- Single-chip stereo filter and codec
- Wide operating voltage range: 2.7 to 5.5 V
- Low-power consumption: 98 mW; 3.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Transparent serial audio data mode in sleep
- IEC 958 digital output
- Peak level detector for start of track detection or VU meter
- Versatile fade processor; slow/fast fade, mute, 12 dB attenuation
- Serial audio interface for I^2S or EIAJ formats
- Error concealment
- Three-wire L3 bus microcontroller interface
- Three sample rates:
  - 32 kHz
  - 44.1 kHz
  - 48 kHz
- Internal or external clock source
- Three programmable outputs
- Small surface mounted package (SOT307).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2003 performs the sub-band filtering and audio frame codec functions in the Precision Adaptive Sub-band Coding (PASC) system. It can be used as a stand-alone decoder for playback only applications, but requires the addition of an Adaptive Allocation and Scale Factor processor (SAA2013) in order to perform PASC encoding in a DCC record system.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2003H	44	QFP[1]	plastic	SOT307

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

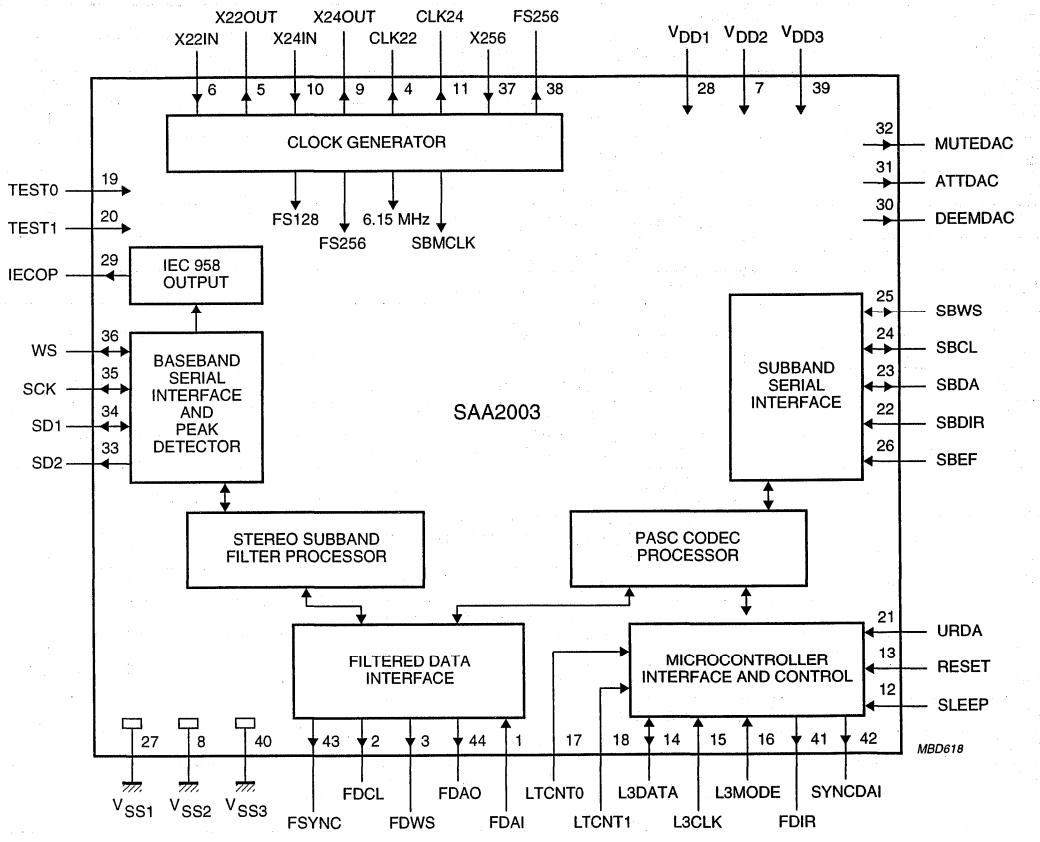


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
FDAI	1	filtered data input from SAA2013	I
FDCL	2	filtered data bit clock	O
FDWS	3	filtered data word select	O
CLK22	4	22.5792 MHz buffered clock output	O
X22OUT	5	22.5792 MHz crystal output	O
X22IN	6	22.5792 MHz crystal input	I
V_{DD2}	7	supply voltage (clock oscillator)	–
V_{SS2}	8	supply ground (clock oscillator)	–
X24OUT	9	24.576 MHz crystal output	O
X24IN	10	24.576 MHz crystal input	I
CLK24	11	24.576 MHz buffered clock output	O
SLEEP	12	sleep mode; device inactive	I
RESET	13	device reset	I
L3DATA	14	3-wire interface; serial data	I/O
L3CLK	15	3-wire interface; bit clock	I
L3MODE	16	3-wire interface; mode control	I
LTCNT0	17	LT interface; control bit 0	I
LTCNT1	18	LT interface; control bit 1	I
TEST0	19	test mode select	I
TEST1	20	test mode select	I
URDA	21	unreliable data flag from drive processor	I
SBDIR	22	sub-band data direction	I
SBDA	23	sub-band serial data	I/O
SBCL	24	sub-band bit clock	I/O
SBWS	25	sub-band word select	I/O
SBEF	26	sub-band error flag from drive processor	I
V_{SS1}	27	digital supply ground	–
V_{DD1}	28	digital supply voltage	–
IECOP	29	IEC 958 digital audio output	O
DEEMDAC	30	DAC control or general purpose output	O
ATTDAC	31	DAC control or general purpose output	O
MUTEDAC	32	DAC control or general purpose output	O
SD2	33	serial audio data to DAC	O
SD1	34	serial audio data to/from DAIO and DAC	I/O
SCK	35	serial audio data bit clock	I/O
WS	36	serial audio data word select	I/O
X256	37	master audio clock from external source	I
FS256	38	master audio clock at 256 times sample frequency	O
V_{DD3}	39	supply voltage (FS256)	–
V_{SS3}	40	supply ground (FS256)	–

SYMBOL	PIN	DESCRIPTION	TYPE
FDIR	41	filter direction; encode or decode	O
SYNCDAI	42	settings synchronization for DAIO	O
FSYNC	43	sub-band 0 sample synchronization for SAA2013	O
FDAO	44	filtered data output to SAA2013	O

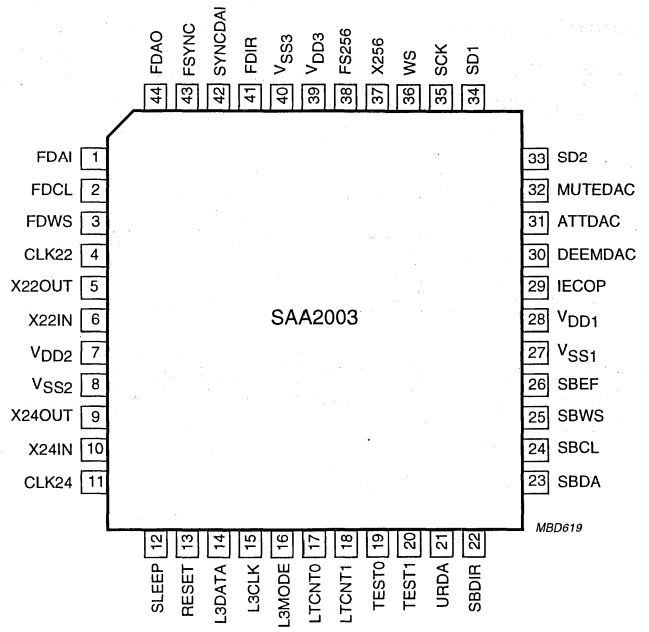


Fig.2 Pin configuration.

Adaptive allocation and scaling for PASC coding in DCC systems

SAA2013

FEATURES

- Wide operating voltage range: 2.7 to 5.5 V
- Low power consumption: 13 mW; 3.0 V
- Low power decode mode: 1 mW; 5.0 V
- Sleep mode for low power and low Electromagnetic Interference (EMI)
- Sophisticated allocation algorithm
- Optimum sound quality
- Three-wire L3 bus microcontroller interface
- Stereo or 2-channel mono recording
- Small surface mounted package (QFP; SOT307).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The SAA2013 performs the adaptive allocation and scaling function in the Precision Adaptive Sub-band Coding (PASC) system. It is not required in playback only applications, and is only used during recording. To complete the PASC processor, a SAA2003 stereo filter and codec is required.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2013H	44	QFP[1]	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

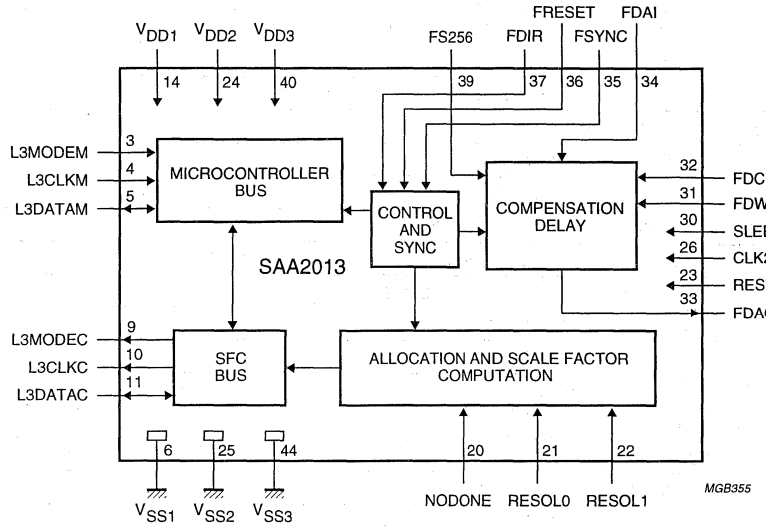


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
TEST10	1	test input; connect to V_{SS}	I
TEST11	2	test input; connect to V_{SS}	I
L3MODEM	3	microcontroller interface mode input	I
L3CLKM	4	microcontroller interface clock input	I
L3DATAM	5	microcontroller interface data 3-state input/output	I/O
V_{SS1}	6	supply ground	–
TEST12	7	test output; do not connect	O
TEST13	8	test output; do not connect	O
L3MODEC	9	codec interface mode output	O
L3CLKC	10	codec interface clock output	O
L3DATAC	11	codec interface data 3-state input/output	I/O
TEST1	12	test output; do not connect	O
TEST2	13	test output; do not connect	O
V_{DD1}	14	supply voltage	–
TEST3	15	test mode input; connect to V_{DD}	I
TEST4	16	test mode input; connect to V_{DD}	I
TEST5	17	test input; connect to V_{SS}	I
TEST6	18	test input; connect to V_{SS}	I
TEST7	19	test input; connect to V_{SS}	I
NODONE	20	nodone state selection input; connect to V_{DD}	I
RESOL0	21	resolution selection 0 input	I
RESOL1	22	resolution selection 1 input	I
RESET	23	reset input; active HIGH	I
V_{DD2}	24	supply voltage	–
V_{SS2}	25	supply ground	–
CLK24	26	24.576 MHz clock input	I
LOWPWR	27	low power decode select input	I
POR	28	power on reset input	I
TEST8	29	test input; connect to V_{SS}	I
SLEEP	30	sleep mode select input	I
FDWS	31	filtered data word select	I
FDCL	32	filtered data clock	I
FDAO	33	filtered data output	O
FDAI	34	filtered data input	I
FSYNC	35	sub-band synchronization on filtered I^2S bus	I
FRESET	36	reset signal input from SAA2003	I
FDIR	37	filtered data direction input	I
TEST9	38	test input; connect to V_{SS}	I
FS256	39	system clock input; 256 × sample frequency (f_s)	I
V_{DD3}	40	supply voltage	–

SYMBOL	PIN	DESCRIPTION	TYPE
n.c.	41	not connected	–
n.c.	42	not connected	–
n.c.	43	not connected	–
V_{SS3}	44	supply ground	–

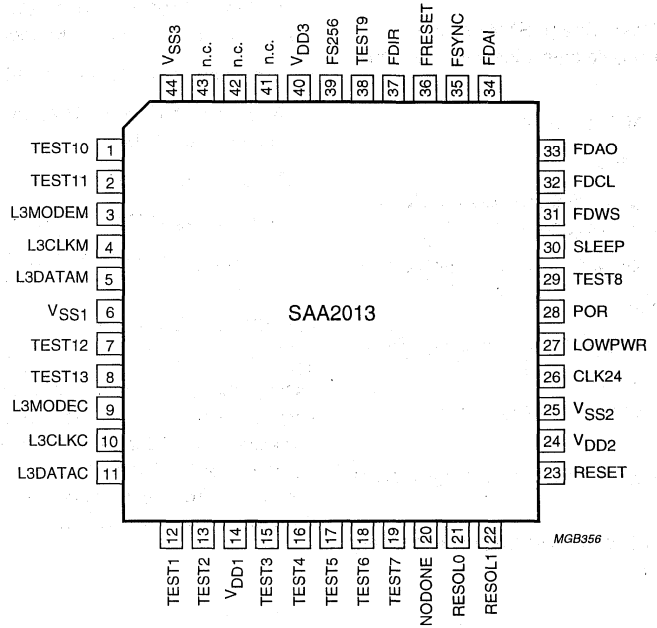


Fig.2 Pin configuration.

Drive processor for DCC systems SAA2023

FEATURES

- Operating supply voltage: 4.5 to 5.5 V
- Low power dissipation: 260 mW at 5.0 V
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording

DIGITAL dcc COMPACT CASSETTE

- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller 'L3' interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA2023 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

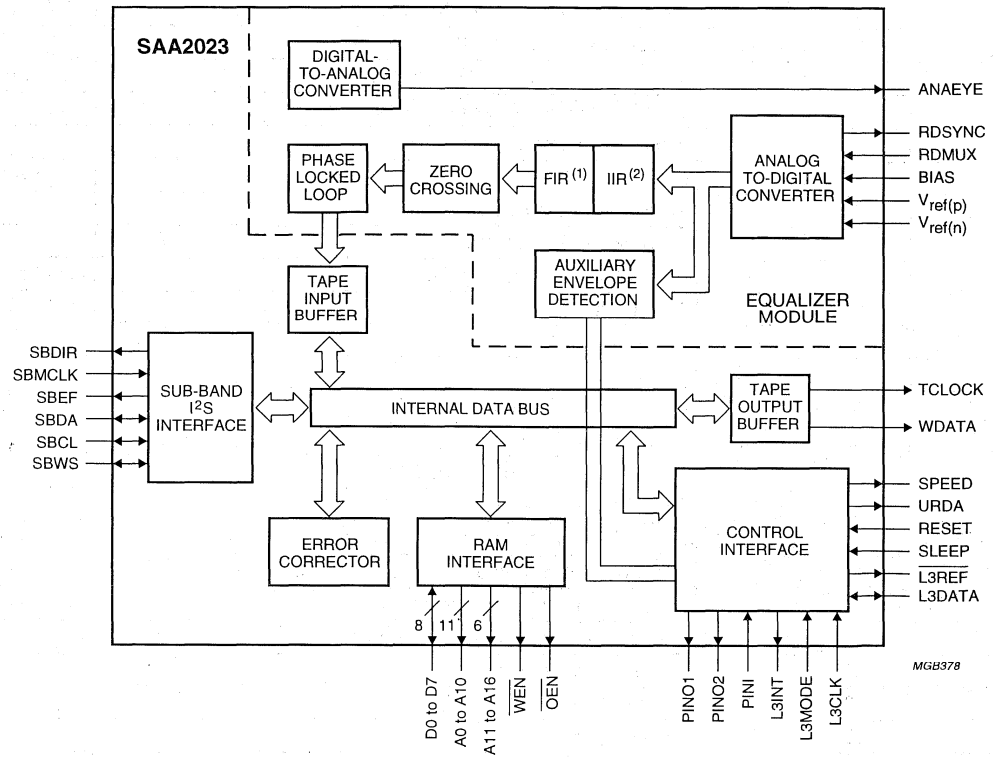
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2023H	80	TQFP80[1]	plastic	SOT315-1
SAA2023GP	80	QFP80[1]	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.
(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{L3REF}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA2023	I
SLEEP	15	13	sleep mode selection of SAA2023	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{OEN}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{RAS}$	22	20	address SRAM; $\overline{RAS}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE(1)
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

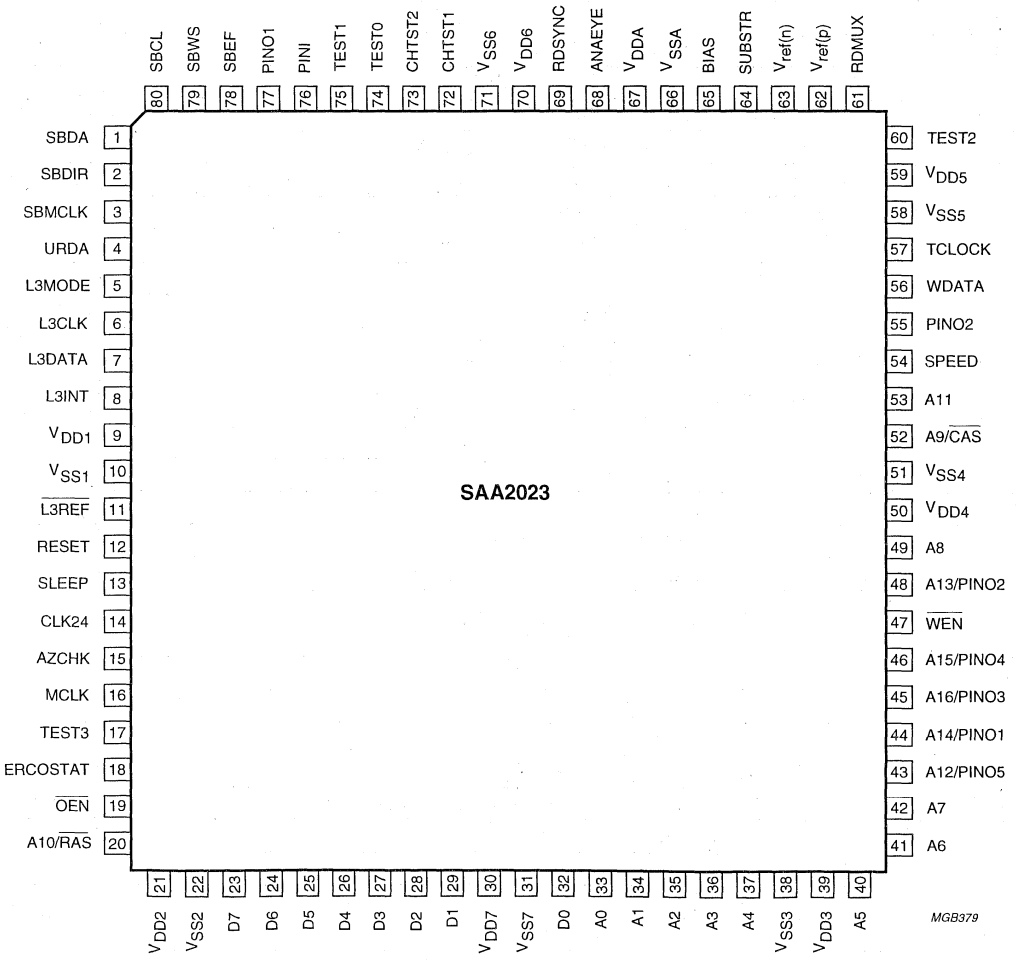


Fig.2 Pin configuration (SOT315-1; TQFP80).

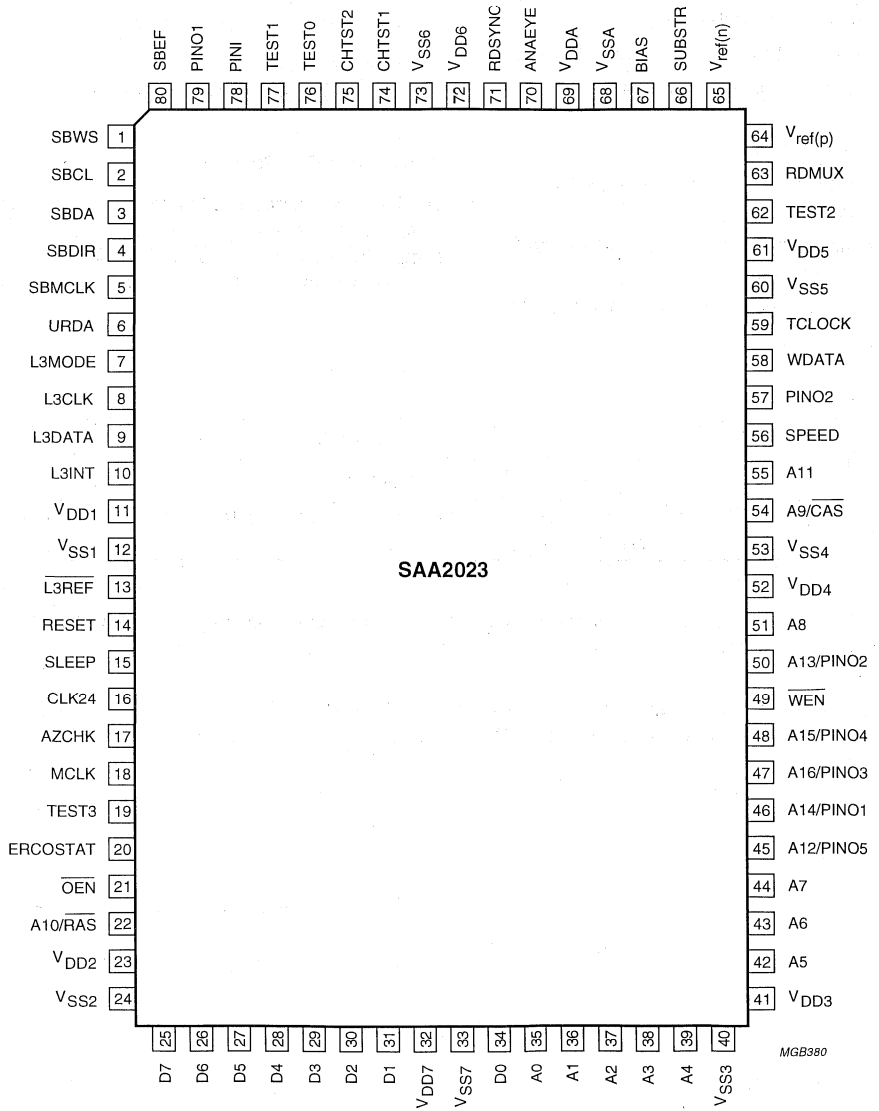


Fig.3 Pin configuration (SOT318-2; QFP80).

MPEG Audio Source Decoder SAA2500

FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and inter-channel crosstalk
- Demultiplexing of ancillary data in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sample frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision; 16, 18, 20 or 22 bit
- Low power consumption.

APPLICATIONS

- Cable and satellite digital radio decoders
- Video CD
- Compact Disc Interactive (CD-I)
- Sold-state audio
- Multimedia Personal Computer (PC).

GENERAL DESCRIPTION

The SAA2500 supports all audio modes (joint stereo, stereo, single channel and dual channel) bit rates and sample frequencies of ISO/MPEG-1 layers I and II, as standardized in *"ISO/IEC 11172-3"*.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2500H	QFP44[1]	Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

Supply of this *"ISO/IEC 11172-3"* audio standard Layer I or layer II compatible IC does not convey a licence nor imply a right under any patent, or any Industrial or Intellectual Property Right, to use this IC in any ready-to-use electronic product.

BLOCK DIAGRAM

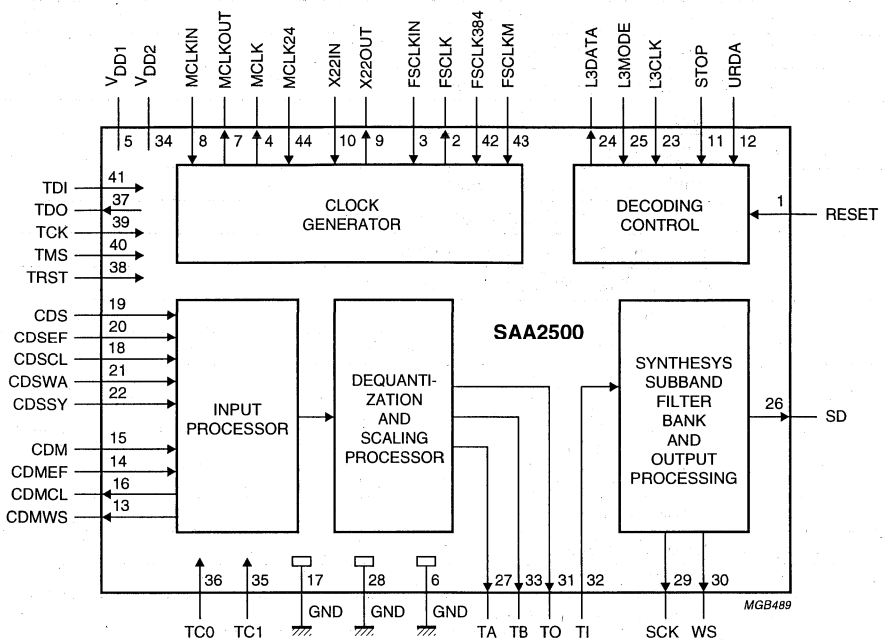


Fig.1 Functional block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	master reset	I
FSCLK	2	sample rate clock; buffered signal	O
FSCLKIN	3	sample rate clock input	I
MCLK	4	master clock; buffered signal	O
V_{DD1}	5	supply voltage	–
GND	6	supply ground	–
MCLKOUT	7	master clock oscillator output	O
MCLKIN	8	master clock oscillator input or signal input	I
X22OUT	9	22.579 MHz clock oscillator output	O
X22IN	10	22.579 MHz clock oscillator input or signal input	I
STOP	11	stop decoding	I
URDA	12	unreliable data input; interrupt decoding	I
CDMWS	13	coded data (master input) word select output	O
CDMEF	14	coded data (master input) error flag input	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	coded data (master input) bit clock output	O
GND	17	supply ground	–
CDSCL	18	coded data (slave input) bit clock	I
CDS	19	ISO/MPEG coded data (slave input)	I
CDSEF	20	coded data (slave input) error flag	I
CDSWA	21	coded data (slave input) window signal	I
CDSSY	22	coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock	I
L3DATA	24	L3 interface serial data	I/O
L3MODE	25	L3 interface address/data select input	I
SD	26	baseband audio I^2S data output	O
TA	27	do not connect; reserved	O
GND	28	supply ground	–
SCK	29	baseband audio data I^2S clock output	O
WS	30	baseband audio data I^2S word select output	O
TO	31	connect to TI (pin 32)	O
TI	32	connect to TO (pin 31)	I
TB	33	do not connect; reserved	O
V_{DD2}	34	supply voltage	–
TC1	35	do not connect; factory test control 1 input, with integrated pull-down resistor	I
TC0	36	do not connect; factory test control 0 input, with integrated pull-down resistor	I
TDO	37	boundary scan test data output	O
TRST	38	boundary scan test reset input; this pin should be connected to ground for normal operation	I
TCK	39	boundary scan test clock input	I

SYMBOL	PIN	DESCRIPTION	TYPE
TMS	40	boundary scan test mode select input	I
TDI	41	boundary scan test data input	I
FSCLK384	42	sample rate clock frequency indication input	I
FSCLKM	43	sample rate clock source selection for the master input	I
MCLK24	44	master clock frequency indication	I

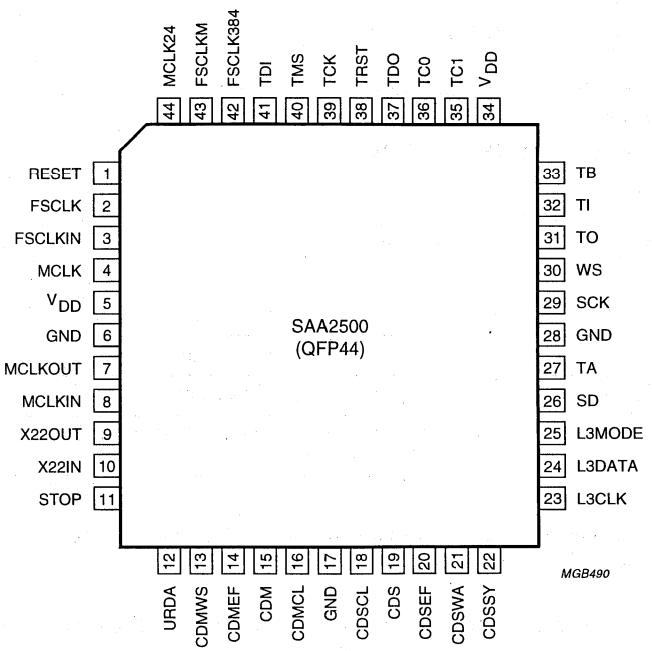


Fig.2 Pin configuration.

1 FEATURES

- Advanced error protection
- Integrated audio post processing for control of signal level and inter-channel crosstalk
- Demultiplexing of Program Associated Data (PAD) in the input bitstream
- Automatic digital de-emphasis of the decoded audio signal
- Separate master and slave inputs
- Automatic sample frequency and bit-rate switching in master input mode
- Automatic synchronization of input and output interface clocks in master input mode
- Selectable audio output precision; 16, 18, 20 or 22 bit
- Low power consumption
- Decoded sub-band signal and error flag outputs for error concealment.

2 APPLICATION

- Digital Audio Broadcast systems as defined in *"Eureka 147"*.

3 GENERAL DESCRIPTION

The SAA2501 audio source decoder supports ISO/IEC MPEG layers I and II and all DAB specific features as described in *"Eureka 147 draft specification (EU147)"*.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA2501H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

Supply of this *"ISO/IEC 11172-3"* audio standard Layer I or layer II compatible IC does not convey a licence nor imply a right under any patent, or any Industrial or Intellectual Property Right, to use this IC in any ready-to-use electronic product.

5 BLOCK DIAGRAM

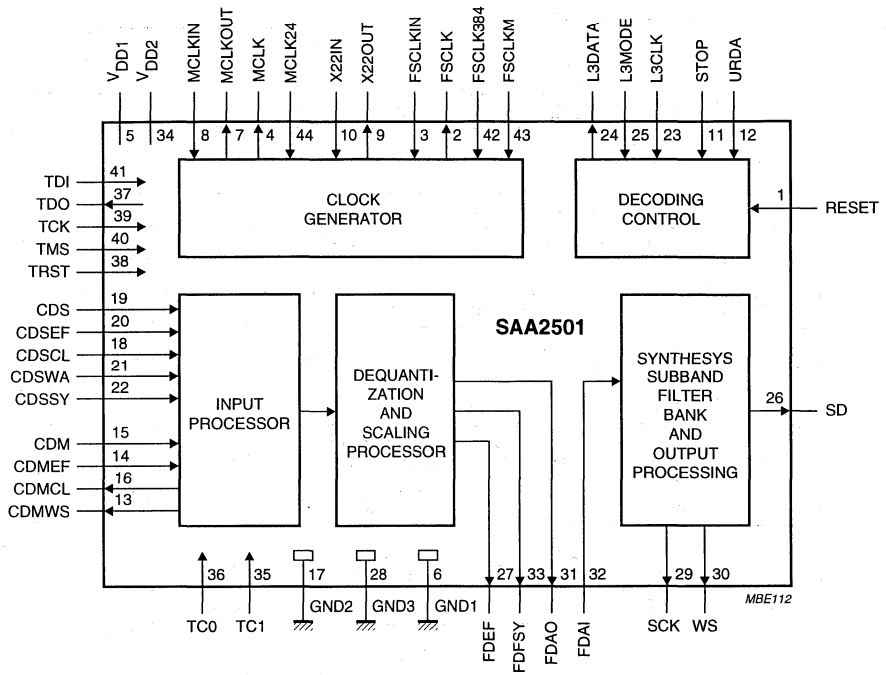


Fig.1 Functional block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
RESET	1	master reset input	I
FSCLK	2	sample rate clock output; buffered signal	O
FSCLKIN	3	sample rate clock signal input (see Table 1)	I
MCLK	4	master clock output; buffered signal	O
V_{DD1}	5	supply voltage 1	–
GND1	6	ground 1	–
MCLKOUT	7	master clock oscillator output	O
MCLKIN	8	master clock oscillator input or signal input	I
X22OUT	9	22.579 MHz clock oscillator output	O
X22IN	10	22.579 MHz clock oscillator input or signal input	I
STOP	11	stop decoding input	I
URDA	12	unreliable data input; interrupt decoding	I
CDMWS	13	coded data (master input) word select output	O
CDMEF	14	coded data (master input) error flag input	I
CDM	15	ISO/MPEG coded data (master input)	I
CDMCL	16	coded data (master input) bit clock output	O
GND2	17	ground 2	–
CDSCL	18	coded data (slave input) bit clock	I
CDS	19	ISO/MPEG or EU147 (see Table 8) coded data (slave input)	I
CDSEF	20	coded data (slave input) error flag	I
CDSWA	21	coded data (slave input) burst window signal	I
CDSSY	22	coded data (slave input) frame sync	I
L3CLK	23	L3 interface bit clock input	I
L3DATA	24	L3 interface serial data input/output	I/O
L3MODE	25	L3 interface address/data select input	I
SD	26	baseband audio I^2S data output	O
FDEF	27	filter data error flag output	O
GND3	28	ground 3	–
SCK	29	baseband audio data I^2S clock output	O
WS	30	baseband audio data I^2S word select output	O
FDAO	31	filter data output	O
FDAI	32	filter data input	I
FDFSY	33	filter data output frame sync	O
V_{DD2}	34	supply voltage 2	–
TC1	35	do not connect; factory test control 1 input, with integrated pull-down resistor	I
TC0	36	do not connect; factory test control 0 input, with integrated pull-down resistor	I
TDO	37	boundary scan test data output	O
TRST	38	boundary scan test reset input; this pin should be connected to ground for normal operation	I
TCK	39	boundary scan test clock input	I

SYMBOL	PIN	DESCRIPTION	TYPE
TMS	40	boundary scan test mode select input	I
TDI	41	boundary scan test data input	I
FSCLK384	42	sample rate clock frequency indication input	I
FSCLKM	43	sample rate clock source selection for the master input	I
MCLK24	44	master clock frequency indication input	I

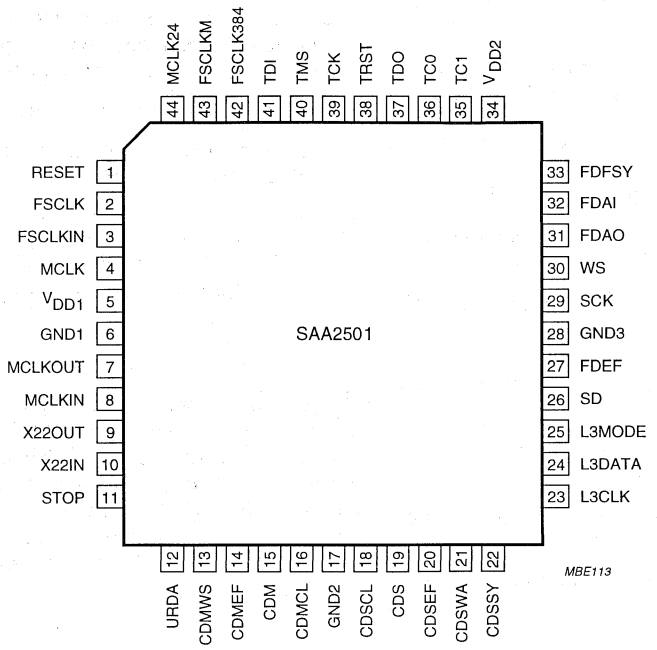


Fig.2 Pin configuration (QFP44).

Drive processor for DCC systems SAA3323

FEATURES

- Operating supply voltage: 2.7 to 3.6 V
- Low power dissipation: 84 mW (typ)
- Single chip digital equalizer, tape formatting and error correction
- 8-bit flash analog-to-digital converter (ADC) for low symbol error rate
- Two switchable Infinite Impulse-Response (IIR) filter sections
- 10-tap Finite Impulse-Response (FIR) filter per main data channel, with 8 bit coefficients, identical for all main channels
- 10-tap FIR filter for the AUX channel
- Analog and digital eye outputs
- Interrupt line triggered by internal auxiliary envelope processing e.g. label, counter, and others
- Robust programmable digital PLL clock extraction unit
- Low power SLEEP mode
- Slew rate limited Electromagnetic Compatibility (EMC) friendly output
- Digital Compact Cassette (DCC) optimized error correction
- Programmable symbol synchronization strategy for tape input data
- Microcontroller control of capstan servo possible during playback and recording

- Frequency and phase regulation of capstan servo during playback
- Choice of Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM) types for system Random Access Memory (RAM)
- Scratch pad RAM for microcontroller in system RAM
- Integrated interface for Precision Adaptive Sub-band Coding (PASC) data bus
- Three wire microcontroller 'L3' interface
- Protection against invalid auxiliary data
- Seamless joins between recordings.

GENERAL DESCRIPTION

The SAA3323 performs the drive processor function in the DCC system. This function is built up of digital equalizer, error correction and tape formatting functions. The digital equalizer is intended for use with DCC read amplifiers TDA1318 or TDA1380. The tape formatting and error correction circuit is intended for use with PASC ICs SAA2003 and SAA2013, and write amplifiers TDA1319 or TDA1381.

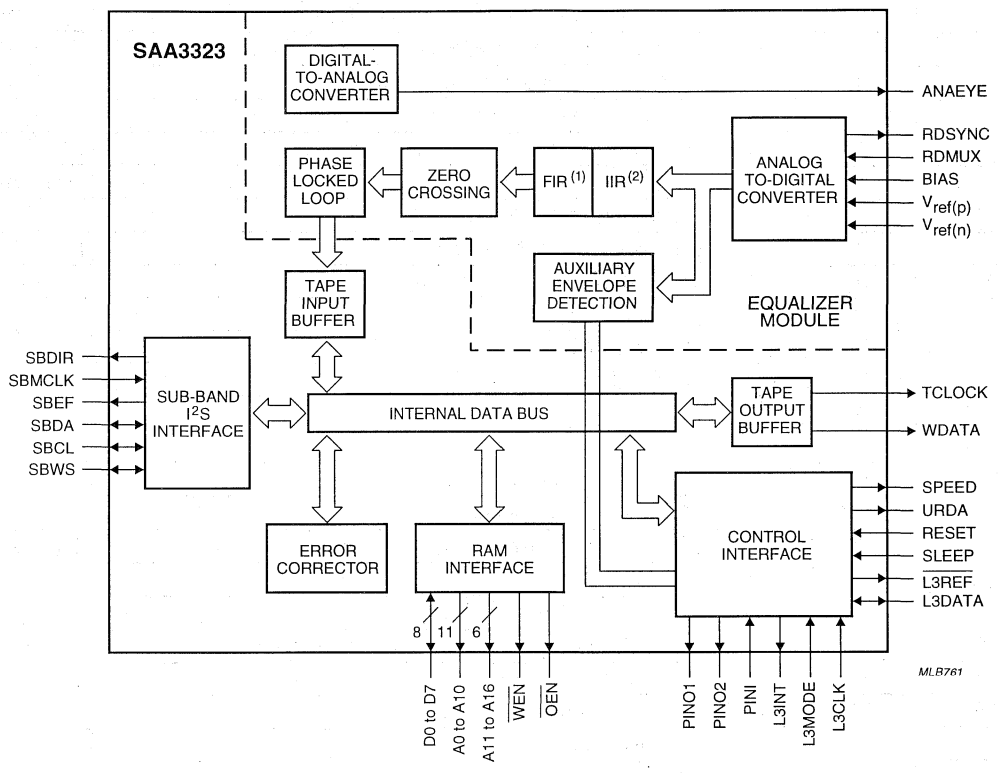
ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA3323H	80	TQFP80[1]	plastic	SOT315-1
SAA3323GP	80	QFP80[1]	plastic	SOT318-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM



(1) FIR = Finite Impulse-Response.
(2) IIR = Infinite Impulse-Response.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
SBWS	1	79	word select for sub-band PASC interface	I/O (1 mA)
SBCL	2	80	bit clock for sub-band PASC interface	I/O (1 mA)
SBDA	3	1	data line for sub-band PASC interface	I/O (1 mA)
SBDIR	4	2	direction line for sub-band PASC interface	O (1 mA)
SBMCLK	5	3	master clock for sub-band PASC interface	I
URDA	6	4	unreliable data	O (1 mA)
L3MODE	7	5	mode line for L3 interface	I
L3CLK	8	6	bit clock line for L3 interface	I
L3DATA	9	7	serial data line for L3 interface	I/O (2 mA)
L3INT	10	8	L3 interrupt output	O (1 mA)
V_{DD1}	11	9	digital supply voltage	S
V_{SS1}	12	10	digital ground	S
$\overline{L3REF}$	13	11	L3 bus timing reference	O (1 mA)
RESET	14	12	reset SAA3323	I
SLEEP	15	13	sleep mode selection of SAA3323	I
CLK24	16	14	24.576 MHz clock input	I
AZCHK	17	15	channel 0 and channel 7 azimuth monitor	O (1 mA)
MCLK	18	16	6.144 MHz clock output	O (1 mA)
TEST3	19	17	TEST3 output; do not connect	O (1 mA)
ERCOSTAT	20	18	ERCO status, for symbol error rate measurements	O (1 mA)
$\overline{OEN}$	21	19	output enable for RAM	O (2 mA)
A10/$\overline{RAS}$	22	20	address SRAM; $\overline{RAS}$ DRAM	O (2 mA)
V_{DD2}	23	21	digital supply voltage	S
V_{SS2}	24	22	digital ground	S
D7	25	23	data SRAM	I/O (4 mA)
D6	26	24	data SRAM	I/O (4 mA)
D5	27	25	data SRAM	I/O (4 mA)
D4	28	26	data SRAM	I/O (4 mA)
D3	29	27	data SRAM; data DRAM	I/O (4 mA)
D2	30	28	data SRAM; data DRAM	I/O (4 mA)
D1	31	29	data SRAM; data DRAM	I/O (4 mA)
V_{DD7}	32	30	digital supply voltage for RAM	S
V_{SS7}	33	31	digital ground for RAM	S
D0	34	32	data SRAM; data DRAM	I/O (4 mA)
A0	35	33	address SRAM; address DRAM	O (2 mA)
A1	36	34	address SRAM; address DRAM	O (2 mA)
A2	37	35	address SRAM; address DRAM	O (2 mA)
A3	38	36	address SRAM; address DRAM	O (2 mA)

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
A4	39	37	address SRAM; address DRAM	O (2 mA)
V_{SS3}	40	38	digital ground	S
V_{DD3}	41	39	digital supply voltage	S
A5	42	40	address SRAM; address DRAM	O (2 mA)
A6	43	41	address SRAM; address DRAM	O (2 mA)
A7	44	42	address SRAM; address DRAM	O (2 mA)
A12/PINO5	45	43	address SRAM; Port expander output 5	O (2 mA)
A14/PINO1	46	44	address SRAM; Port expander output 1	O (2 mA)
A16/PINO3	47	45	address SRAM; Port expander output 3	O (2 mA)
A15/PINO4	48	46	address SRAM; Port expander output 4	O (2 mA)
$\overline{WEN}$	49	47	write enable for RAM	O (2 mA)
A13/PINO2	50	48	address SRAM; Port expander output 2	O (2 mA)
A8	51	49	address SRAM; address DRAM	O (2 mA)
V_{DD4}	52	50	digital supply voltage	S
V_{SS4}	53	51	digital ground	S
A9/$\overline{CAS}$	54	52	address SRAM; $\overline{CAS}$ for DRAM	O (2 mA)
A11	55	53	address SRAM	O (2 mA)
SPEED	56	54	Pulse Width Modulation (PWM) capstan control output for deck	O_t (1 mA)
PINO2	57	55	Port expander output 2	O_t (1 mA)
WDATA	58	56	serial output to write amplifier	O (1 mA)
TCLOCK	59	57	3.072 MHz clock output for tape I/O	O (1 mA)
V_{SS5}	60	58	digital ground	S
V_{DD5}	61	59	digital supply voltage	S
TEST2	62	60	TEST mode select; do not connect	I_{pd}
RDMUX	63	61	analog multiplexed input from read amplifier	I_A
$V_{ref(p)}$	64	62	ADC positive reference voltage	I_A
$V_{ref(n)}$	65	63	ADC negative reference voltage	I_A
SUBSTR	66	64	substrate connection	I_A
BIAS	67	65	bias current for ADC	I_A
V_{SSA}	68	66	analog ground	S
V_{DDA}	69	67	analog supply voltage	S
ANAEYE	70	68	analog eye pattern output	O_A
RDSYNC	71	69	synchronization output for read amplifier	O (1 mA)
V_{DD6}	72	70	digital supply voltage	S
V_{SS6}	73	71	digital ground	S
CHTST1	74	72	channel test pin 1	O (1 mA)
CHTST2	75	73	channel test pin 2	O (1 mA)
TEST0	76	74	TEST mode select; do not connect	I_{pd}
TEST1	77	75	TEST mode select; do not connect	I_{pd}

SYMBOL	PIN		DESCRIPTION	TYPE[1]
	QFP80	TQFP80		
PINI	78	76	Port expander input	I
PINO1	79	77	Port expander output 1	O (1 mA)
SBEF	80	78	sub-band PASC error flag line	O (1 mA)

Note

1. I = input; I_A = analog input; I_{pd} = input with pull-down resistance; I/O = bidirectional; O = output; O_A = analog output; O_t = 3-state output; S = supply.

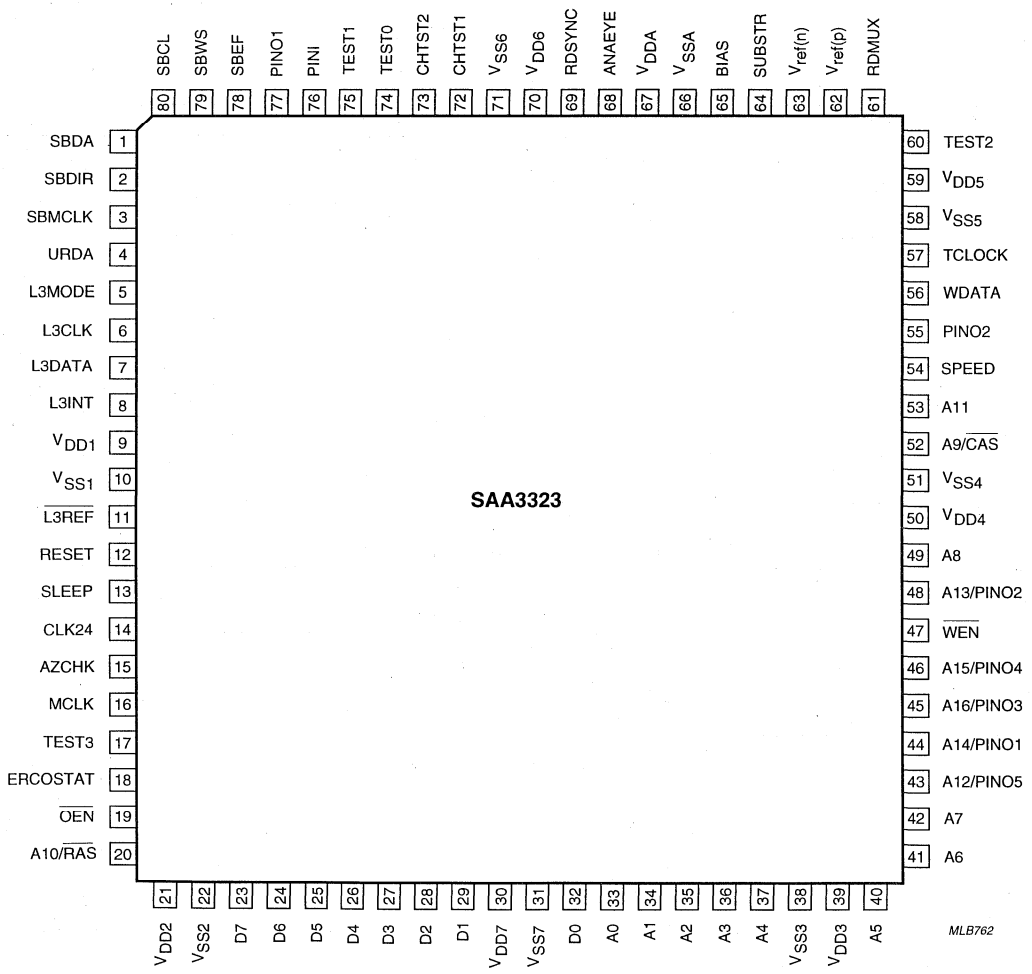


Fig.2 Pin configuration (SOT315-1; TQFP80).

Digital Video Encoder (EURO-DENC) SAA7182; SAA7183

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC/SECAM encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port. Input data format Cb, Y, Cr etc. or Y and Cb, Cr on 16 lines (*"CCIR 656"*)
- Three DACs for CVBS, Y and C operating at 27 MHz with 10-bit resolution
- Three DACs for RGB operating at 27 MHz with 9-bit resolution, RGB sync on CVBS and Y
- CVBS, Y, C and RGB output simultaneously
- Closed captioning and teletext encoding including sequencer and filter
- On-chip YUV to RGB matrix
- Fast I²C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Macrovision Pay-per-View protection system as option, also used for RGB output

  This applies to SAA7183 only. The device is protected by USA patent numbers 461603, 4577216 and 4819098 and other intellectual property rights.

  Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductor sales office for more information
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- PLCC84 package.

GENERAL DESCRIPTION

The SAA7182; SAA7183 encodes digital YUV video data to an NTSC, PAL, SECAM CVBS or S-Video signal and also RGB.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.75	5.0	5.25	V
I_{DDA}	analog supply current	–	90	110	mA
I_{DDD}	digital supply current	–	220	250	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C, CVBS and RGB without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7182WP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2
SAA7183WP	PLCC84	plastic leaded chip carrier; 84 leads	SOT189-2

BLOCK DIAGRAM

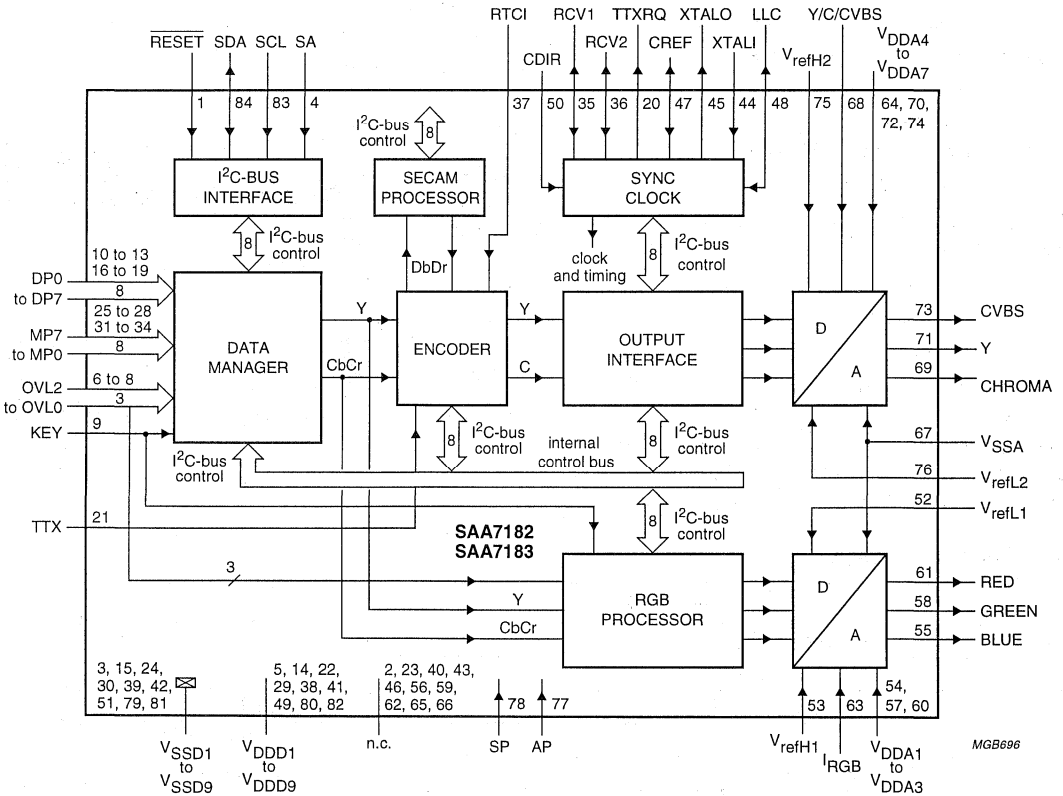


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{\text{RESET}}$	1	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode. The I²C-bus receiver waits for the START condition.
n.c.	2	not connected
V_{SSD1}	3	digital ground 1
SA	4	The I²C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{DDD1}	5	digital supply voltage 1
OVL2	6	3-bit overlay data input. This is the index for the internal look-up table.
OVL1	7	
OVL0	8	
KEY	9	Key input for OVL. When HIGH it selects OVL input.
DP0	10	Lower 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP1	11	
DP2	12	
DP3	13	
V_{DDD2}	14	digital supply voltage 2
V_{SSD2}	15	digital ground 2
DP4	16	Upper 4 bits of the data port. Input for multiplexed Cb, Cr data if 16 line input mode is used.
DP5	17	
DP6	18	
DP7	19	
TTXRQ	20	Teletext request output, indicating when the bitstream is valid.
TTX	21	Teletext bitstream input.
V_{DDD3}	22	digital supply voltage 3
n.c.	23	not connected
V_{SSD3}	24	digital ground 3
MP7	25	Upper 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data, or input for Y data only, if 16 line input mode is used.
MP6	26	
MP5	27	
MP4	28	
V_{DDD4}	29	digital supply voltage 4
V_{SSD4}	30	digital ground 4
MP3	31	Lower 4 bits of MPEG port. It is an input for *"CCIR 656"* style multiplexed Cb, Y, Cr data, or input for Y data only, if 16 line input mode is used.
MP2	32	
MP1	33	
MP0	34	
RCV1	35	Raster Control 1 for video port. This pin receives/provides a VS/FS/FSEQ signal.
RCV2	36	Raster Control 2 for video port. This pin provides an HS pulse of programmable length or receives an HS pulse.
RTCI	37	Real Time Control Input. If the LLC clock is provided by an *SAA7111* or *SAA7151B*, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality.

SYMBOL	PIN	DESCRIPTION
V_{DDD5}	38	digital supply voltage 5
V_{SSD5}	39	digital ground 5
n.c.	40	not connected
V_{DDD6}	41	digital supply voltage 6
V_{SSD6}	42	digital ground 6
n.c.	43	not connected
XTALI	44	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should be connected to ground.
XTALO	45	Crystal oscillator output (to crystal).
n.c.	46	not connected
CREF	47	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
LLC	48	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The I/O direction is set by the CDIR pin.
V_{DDD7}	49	digital supply voltage 7
CDIR	50	Clock direction. If the CDIR input is HIGH, the circuit receives a clock and optional CREF signal, otherwise if CDIR is LOW CREF and LLC are generated by the internal crystal oscillator.
V_{SSD7}	51	digital ground 7
V_{refL1}	52	Lower reference voltage 1 input for the RGB DACs, connect to V_{SSA}.
V_{refH1}	53	Upper reference voltage 1 input for the RGB DACs, connect via 100 nF capacitor to V_{SSA}.
V_{DDA1}	54	Analog supply voltage 1 for the RGB DACs.
BLUE	55	Analog output of the BLUE component.
n.c.	56	not connected
V_{DDA2}	57	Analog supply voltage 2 for the RGB DACs.
GREEN	58	Analog output of the GREEN component.
n.c.	59	not connected
V_{DDA3}	60	Analog supply voltage 3 for the RGB DACs.
RED	61	Analog output of the RED component.
n.c.	62	not connected
I_{RGB}	63	Current input for RGB amplifiers, connected via 15 kΩ resistor to V_{DDA}.
V_{DDA4}	64	Analog supply voltage 4 for the Y/C/CVBS DACs.
n.c.	65	not connected
n.c.	66	not connected
V_{SSA}	67	Analog ground for the DACs.
$I_{Y/C/CVBS}$	68	Current input for the Y/C/CVBS amplifiers, connected via 15 kΩ resistor to V_{DDA}.
CHROMA	69	Analog output of the chrominance signal.
V_{DDA5}	70	Analog supply voltage 5 for the Y/C/CVBS DACs.
Y	71	Analog output of the luminance signal.
V_{DDA6}	72	Analog supply voltage 6 for the Y/C/CVBS DACs.
CVBS	73	Analog output of the CVBS signal.

SYMBOL	PIN	DESCRIPTION
V_{DDA7}	74	Analog supply voltage 6 for the Y/C/CVBS DACs.
V_{refH2}	75	Upper reference voltage 2 input for the Y/C/CVBS DACs, connected via 100 nF capacitor to V_{SSA}.
V_{refL2}	76	Lower reference voltage 2 input for the Y/C/CVBS DACs, connect to V_{SSA}.
AP	77	Test pin. Connected to digital ground for normal operation.
SP	78	Test pin. Connected to digital ground for normal operation.
V_{SSD8}	79	digital ground 8
V_{DDD8}	80	digital supply voltage 8
V_{SSD9}	81	digital ground 9
V_{DDD9}	82	digital supply voltage 9
SCL	83	I^2C-bus serial clock input.
SDA	84	I^2C-bus serial data input/output.

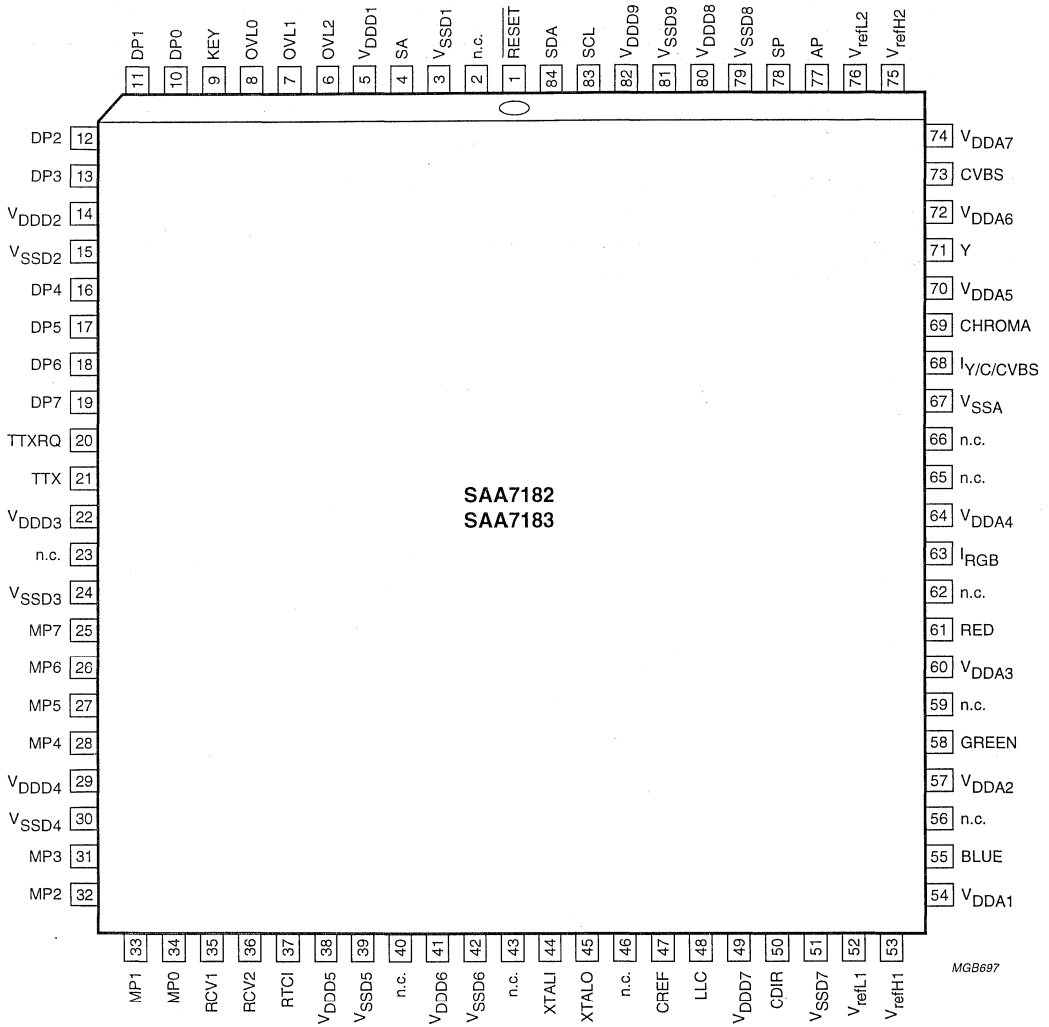


Fig.2 Pin configuration.

Digital Video Encoder (DENC2) SAA7185

FEATURES

- CMOS 5 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data
- 8-bit wide MPEG port
- Input data format Cb, Y, Cr etc. (CCIR 656)
- 16-bit wide YUV input port
- I²C-bus control or alternatively MPU parallel control port
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- OSD overlay with Look-Up Tables (LUTs) 8 × 3 bytes
- Colour bar generator
- Line 21 Closed Caption encoder
- Cross-colour reduction
- DACs operating at 27 MHz with 10-bit resolution
- Controlled rise/fall times of output syncs and blanking
- Down-mode of DACs
- CVBS and S-Video output simultaneously
- PLCC68 package.

GENERAL DESCRIPTION

The SAA7185 encodes digital YUV video data to an NTSC, PAL CVBS or S-Video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip Digital-to-Analog Converters (DACs).

The circuit is compatible to the DIG-TV2 chip family.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	4.75	5.0	5.25	V
V_{DDD}	digital supply voltage	4.5	5.0	5.5	V
I_{DDA}	analog supply current	–	50	55	mA
I_{DDD}	digital supply current	–	140	170	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	2	–	V
R_L	load resistance	80	–	–	Ω
ILE	LF integral linearity error	–	–	±2	LSB
DLE	LF differential linearity error	–	–	±1	LSB
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7185WP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

BLOCK DIAGRAM

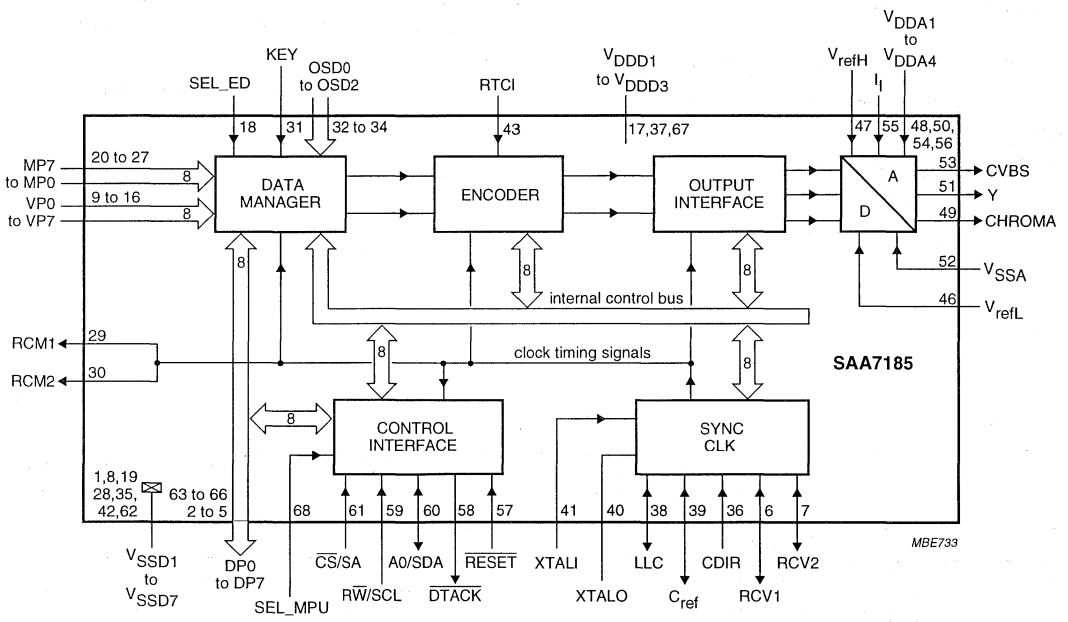


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSD1}	1	digital ground 1
DP4	2	Upper 4 bits of the Data Port. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, they are the UV lines of the Video Port.
DP5	3	
DP6	4	
DP7	5	
RCV1	6	Raster Control 1 for Video port. Depending on the synchronization mode, this pin receives/provides a VS/FS/FSEQ signal.
RCV2	7	Raster Control 2 for Video port. Depending on the synchronization mode, this pin receives/provides an HS/HREF/CBL signal.
V_{SSD2}	8	digital ground 2
VP0	9	Video Port. This is an input for CCIR 656 compatible, multiplexed video data. If the 16-bit DIG-TV2 format is used, this is the Y data.
VP1	10	
VP2	11	
VP3	12	
VP4	13	
VP5	14	
VP6	15	
VP7	16	
V_{DDD1}	17	digital supply voltage 1
SEL_ED	18	Select Encoder Data. Selects data either from MPEG port or from video port as encoder input.
V_{SSD3}	19	digital ground 3
MP7	20	MPEG Port. It is an input for CCIR 656 style multiplexed YUV data.
MP6	21	
MP5	22	
MP4	23	
MP3	24	
MP2	25	
MP1	26	
MP0	27	
V_{SSD4}	28	digital ground 4
RCM1	29	Raster Control 1 for MPEG port. This pin provides a VS/FS/FSEQ signal.
RCM2	30	Raster Control 2 for MPEG port. This pin provides an HS pulse for the MPEG decoder.
KEY	31	Key signal for OSD. It is active HIGH.
OSD0	32	On-Screen Display data. This is the index for the internal OSD look-up table.
OSD1	33	
OSD2	34	
V_{SSD5}	35	digital ground 5
CDIR	36	Clock direction. If the CDIR input is HIGH, the circuit receives a clock signal, otherwise LLC and CREF are generated by the internal crystal oscillator.
V_{DDD2}	37	digital supply voltage 2

SYMBOL	PIN	DESCRIPTION
LLC	38	Line-Locked Clock. This is the 27 MHz master clock for the encoder. The direction is set by the CDIR pin.
C_{ref}	39	Clock Reference signal. This is the clock qualifier for DIG-TV2 compatible signals.
XTALO	40	Crystal oscillator output (to crystal).
XTALI	41	Crystal oscillator input (from crystal). If the oscillator is not used, this pin should br connected to ground.
V_{SSD6}	42	digital ground 6
RTCI	43	Real Time Control Input. If the clock is provided by an SAA7151B, RTCI should be connected to the RTCO pin of the decoder to improve the signal quality.
AP	44	Test pin. Connect to digital ground for normal operation.
SP	45	Test pin. Connect to digital ground for normal operation.
V_{refL}	46	Lower reference voltage input for the DACs.
V_{refH}	47	Upper reference voltage input for the DACs.
V_{DDA1}	48	Analog positive supply voltage 1 for the DACs and output amplifiers.
CHROMA	49	Analog output of the chrominance signal.
V_{DDA2}	50	Analog supply voltage 2 for the DACs and output amplifiers.
Y	51	Analog output of the luminance signal.
V_{SSA}	52	Analog ground for the DACs and output amplifiers.
CVBS	53	Analog output of the CVBS signal.
V_{DDA3}	54	Analog supply voltage 3 for the DACs and output amplifiers.
I_I	55	Current input for the output amplifiers, connect via a 15 kΩ resistor to V_{DDA}.
V_{DDA4}	56	Analog supply voltage 4 for the DACs and output amplifiers.
$\overline{RESET}$	57	Reset input, active LOW. After reset is applied, all outputs are in 3-state input mode. The I^2C-bus receiver waits for the start condition.
$\overline{DTACK}$	58	Data acknowledge output of the parallel MPU interface, active LOW, otherwise high impedance.
R$\overline{W}$/SCL	59	If pin 68 (SEL_MPU) is HIGH, this is the read/write signal of the parallel MPU interface, otherwise it is the I^2C-bus serial clock input.
A0/SDA	60	If pin 68 (SEL_MPU) is HIGH, this is the address signal of the parallel MPU interface, otherwise it is the I^2C-bus serial data input/output.
$\overline{CS}$/SA	61	If pin 68 (SEL_MPU) is HIGH, this is the chip select signal of the parallel MPU interface, otherwise it is the I^2C-bus slave address select pin. LOW: slave address = 88H, HIGH = 8CH.
V_{SSD7}	62	digital ground 7
DP0	63	Lower 4 bits of the Data Port. If pin 68 (SEL_MPU) is HIGH, this is the data bus of the parallel MPU interface. If it is LOW, they are the UV lines of the Video Port.
DP1	64	
DP2	65	
DP3	66	
V_{DDD3}	67	digital supply voltage 3
SEL_MPU	68	Select MPU interface input. If it is HIGH, the parallel MPU interface is active, otherwise the I^2C-bus interface will be used.

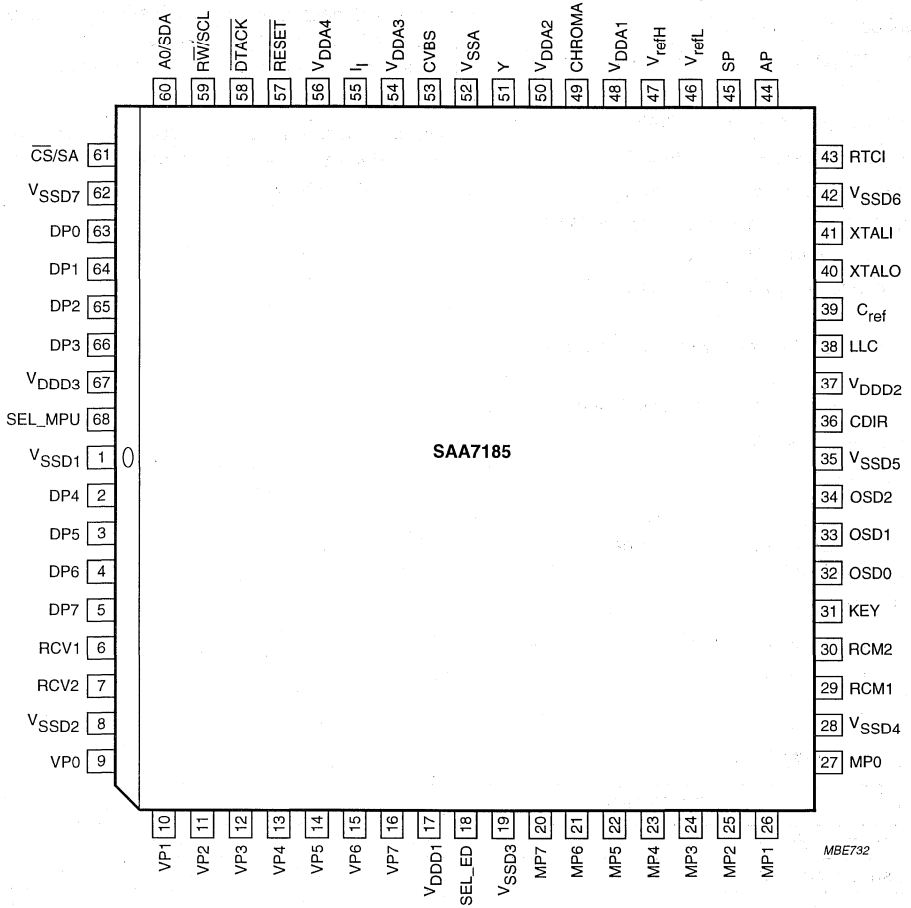


Fig.2 Pin configuration.

CMOS digital decoding IC with RAM for Compact Disc

SAA7345

FEATURES

- Integrated data slicer and clock regenerator
- Digital Phase-Locked Loop (PLL)
- Demodulator and Eight-to-Fourteen Modulation (EFM) decoding
- Subcoding microcontroller serial interface
- Integrated programmable motor speed control
- Error correction and concealment functions
- Embedded Static Random Access Memory (SRAM) for de-interleave and First-In First-Out (FIFO)
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface [European Broadcasting Union (EBU)]
- 2 to 4 times oversampling integrated digital filter
- Audio data peak level detection
- Versatile audio data serial interface
- Digital de-emphasis filter
- Kill interface for Digital-to-Analog Converter (DAC) deactivation during digital silence
- Double speed mode
- Compact Disc Read Only Memory (CD-ROM) modes
- A single speed only version is available (SAA7345GP/SS).

GENERAL DESCRIPTION

The SAA7345 incorporates the CD signal processing functions of decoding and digital filtering. The device is equipped with on-board SRAM and includes additional features to reduce the processing required in the analog domain.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	–	22	50	mA
f_{xtal}	crystal frequency	8	16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature	–40	–	+85	°C
T_{stg}	storage temperature	–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7345GP	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

BLOCK DIAGRAM

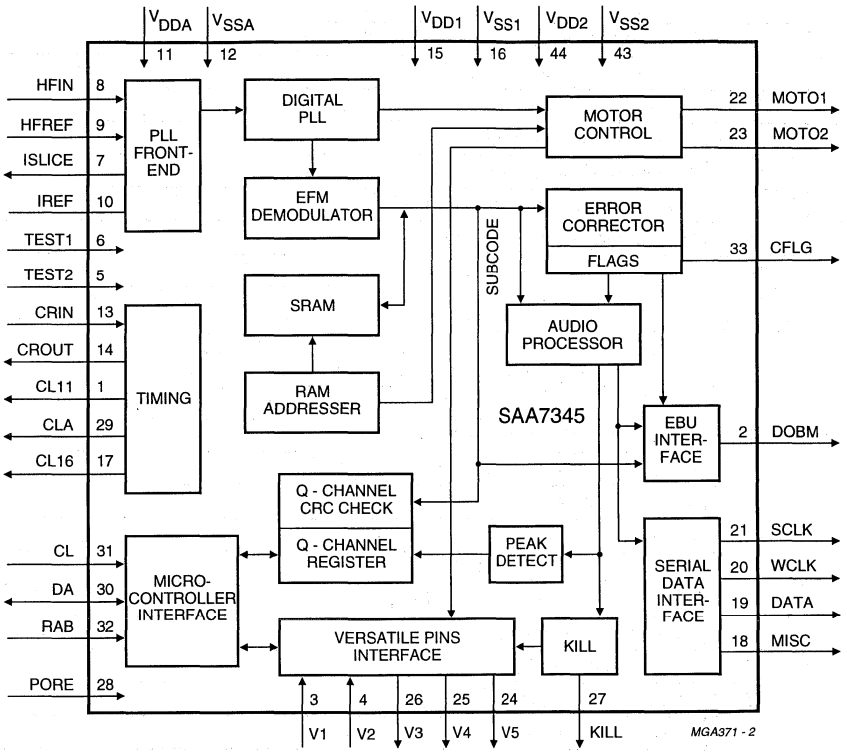


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CL11	1	11.2896 or 5.6448 MHz clock output (3-state); (divide-by-3)
DOBM	2	bi-phase mark output (externally buffered; 3-state)
V1	3	versatile input pin
V2	4	versatile input pin
TEST2	5	test input; this pin should be tied LOW
TEST1	6	test input; this pin should be tied LOW
ISLICE	7	current feedback output from data slicer
HFIN	8	comparator signal input
HFREF	9	comparator common-mode input
IREF	10	reference current pin (nominally $\frac{1}{2}V_{DD}$)
V_{DDA}	11	analog supply voltage; note 1
V_{SSA}	12	analog ground; note 1
CRIN	13	crystal/resonator input
CROUT	14	crystal/resonator output
V_{DD1}	15	digital supply to input and output buffers; note 1
V_{SS1}	16	digital ground to input and output buffers; note 1
CL16	17	16.9344 MHz system clock output
MISC	18	general purpose DAC output (3-state)
DATA	19	serial data output (3-state)
WCLK	20	word clock output (3-state)
SCLK	21	serial bit clock output (3-state)
MOTO1	22	motor output 1; versatile (3-state)
MOTO2	23	motor output 2; versatile (3-state)
V5	24	versatile output pin
V4	25	versatile output pin
V3	26	versatile output pin (open-drain)
KILL	27	kill output; programmable (open-drain)
$\overline{PORE}$	28	power-on reset enable input (active LOW)
CLA	29	4.2336 MHz microcontroller clock output
DA	30	interface data I/O line
CL	31	interface clock input line
RAB	32	interface R/$\overline{W}$ and acknowledge input
CFLG	33	correction flag output (open-drain)
n.c.	34 to 42	no internal connection
V_{SS2}	43	digital ground to internal logic; note 1
V_{DD2}	44	digital supply voltage to internal logic; note 1

Note

1. All supply pins must be connected to the same external power supply.

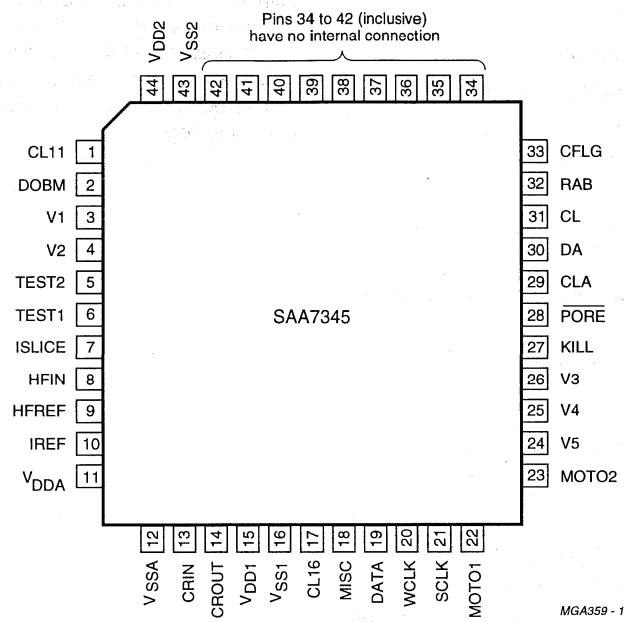


Fig.2 Pin configuration.

Shock absorbing RAM addresser SAA7346

FEATURES

- Absorbs shocks from x, y and z directions
- Absorbs rotational shocks
- Absorbs multiple shocks per second
- Interfaces directly to compact disc decoders SAA7345, SAA7347 and SAA7370
- Multi-speed I^2S-bus input with single-speed I^2S-bus output
- Controls 1 or 4 MBit of external Dynamic Random Access Memory (DRAM)
- Easy serial interface for communication with common microcontrollers
- Software selectable shock detectors
- By-pass/power-down mode
- Kill interface for DAC deactivation
- Can be used for:
  - 'sampling' part of a disc
  - to reduce access pauses between jumps
  - to deliver a programmable delay
  - to generate a fixed audio rate from Constant Angular Velocity (CAV) discs.

GENERAL DESCRIPTION

The SAA7346 can be used to make a CD player insensitive to shocks. To do this, SAA7346 operates closely with a standard 1 Mbit or 4 Mbit DRAM. Audio data is stored inside the DRAM and during shocks the data of the DRAM can be played. The SAA7346 functions as a customized DRAM controller with serial I/O and on-board shock detectors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.3	5.0	5.5	V
I_{DD}	supply current	–	12	–	mA
f_{clk}	clock frequency	–	16.9344	–	MHz
$f_{i(clk)}$	I^2S input word clock frequency	44.1	88.2	176.4	kHz
$f_{o(clk)}$	I^2S output word clock frequency	44.1	88.2	176.4	kHz
T_{amb}	operating ambient temperature	−40	–	+85	°C
T_{stg}	storage temperature	−65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7346H	44	QFP[1]	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocketbook"* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

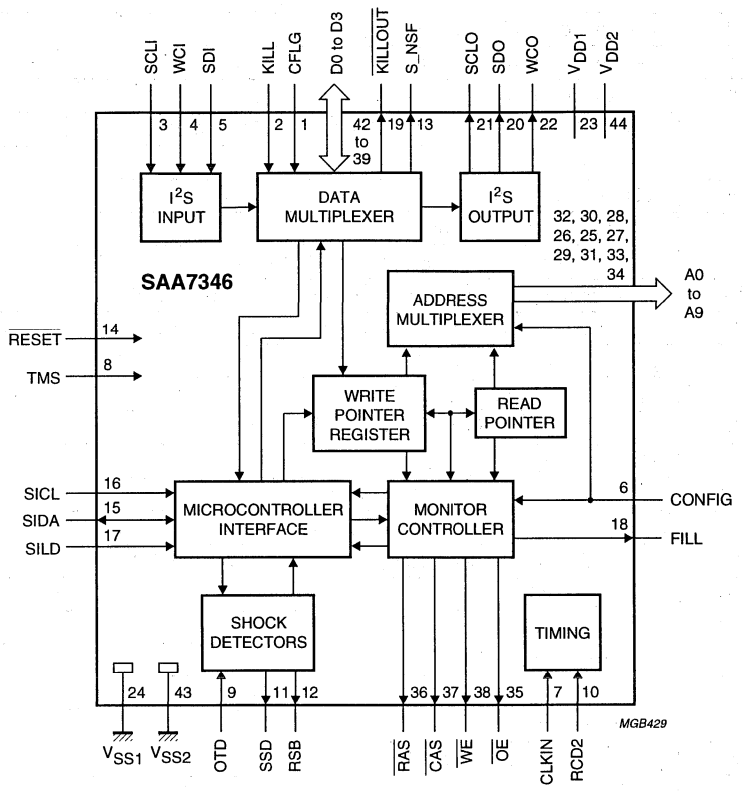


Fig.1 Simplified SAA7347 block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CFLG	1	correction flag input from CD decoder
KILL	2	kill input
SCLI	3	multi-speed I²S bit clock input
WCI	4	multi-speed I²S word clock input
SDI	5	multi-speed I²S data input
CONFIG	6	external DRAM select input; HIGH 4 Mbit, LOW 1 Mbit
CLKIN	7	16.9344 MHz system clock input
TMS	8	test mode select input; active HIGH
OTD	9	on/off track detector input
RCD2	10	DRAM read cycle divide-by-2 input; active HIGH
SSD	11	shock detected output; active HIGH when shock is detected
RSB	12	rotational shock busy output; active HIGH when rotational shock is detected
S_NSF	13	synthetic new subcode frame output
$\overline{\text{RESET}}$	14	reset enable input; active LOW
SIDA	15	microcontroller interface input/output data line
SICL	16	microcontroller interface clock input
SILD	17	microcontroller interface $\overline{\text{read}}$/write input
FILL	18	FIFO write enable output; active HIGH
$\overline{\text{KILLOUT}}$	19	open drain output; active LOW; when in by-pass mode $\overline{\text{KILLOUT}}$ equals KILL
SDO	20	I²S data output
SCLO	21	I²S bit clock output
WCO	22	I²S word clock output
V_{DD1}	23	supply voltage 1
V_{SS1}	24	supply ground 1
A4	25	DRAM address bus output 4
A3	26	DRAM address bus output 3
A5	27	DRAM address bus output 5
A2	28	DRAM address bus output 2
A6	29	DRAM address bus output 6
A1	30	DRAM address bus output 1
A7	31	DRAM address bus output 7
A0	32	DRAM address bus output 0
A8	33	DRAM address bus output 8
A9	34	DRAM address bus output 9
$\overline{\text{OE}}$	35	DRAM enable output; active LOW
$\overline{\text{RAS}}$	36	DRAM row address strobe output; active LOW
$\overline{\text{CAS}}$	37	DRAM column address strobe output; active LOW
$\overline{\text{WE}}$	38	DRAM write enable output; active LOW

SYMBOL	PIN	DESCRIPTION
D3 to D0	39 to 42	DRAM data bus inputs/outputs
V_{SS2}	43	supply ground 2
V_{DD2}	44	supply voltage 2

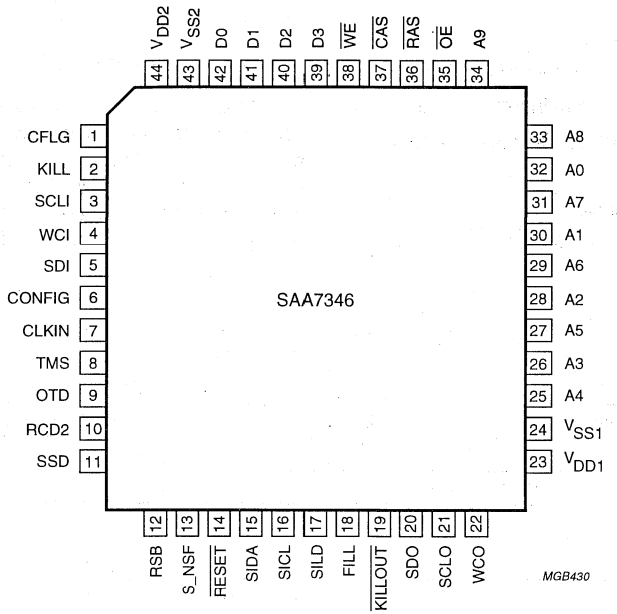


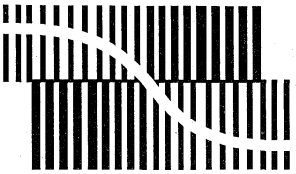
Fig.2 Pin configuration.

Bitstream conversion ADC for digital audio systems

SAA7360

FEATURES

- Stereo input
- Single-ended input
- Uncommitted input buffer for filtering and pre-scaling
- Fully differential analog-to-digital converter (ADC) using 3rd order Sigma-Delta modulation
- 128 times oversampling
- Four stage digital decimation filter
- Switchable high-pass filter to remove DC offsets
- 16-bit or 18-bit selectable output in a multiple of formats
- Sampling rates between 18 and 53 kHz supported
- Master or slave operation
- Choice of 2 crystal frequencies
- Single power supply operation (+5 V).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7360 is a CMOS ADC using Philips bitstream conversion technique. The device is designed for digital audio playback systems, such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). The device is a complementary device to the SAA7350 bitstream conversion digital-to-analog converter (DAC).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
f_{xtal}	crystal frequency	$256f_s$	–	11.2896	–	MHz
		$512f_s$	–	22.5792	–	MHz
THD + N	total harmonic distortion + noise		–	–90	–85	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7360GP	QFP44[1]	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

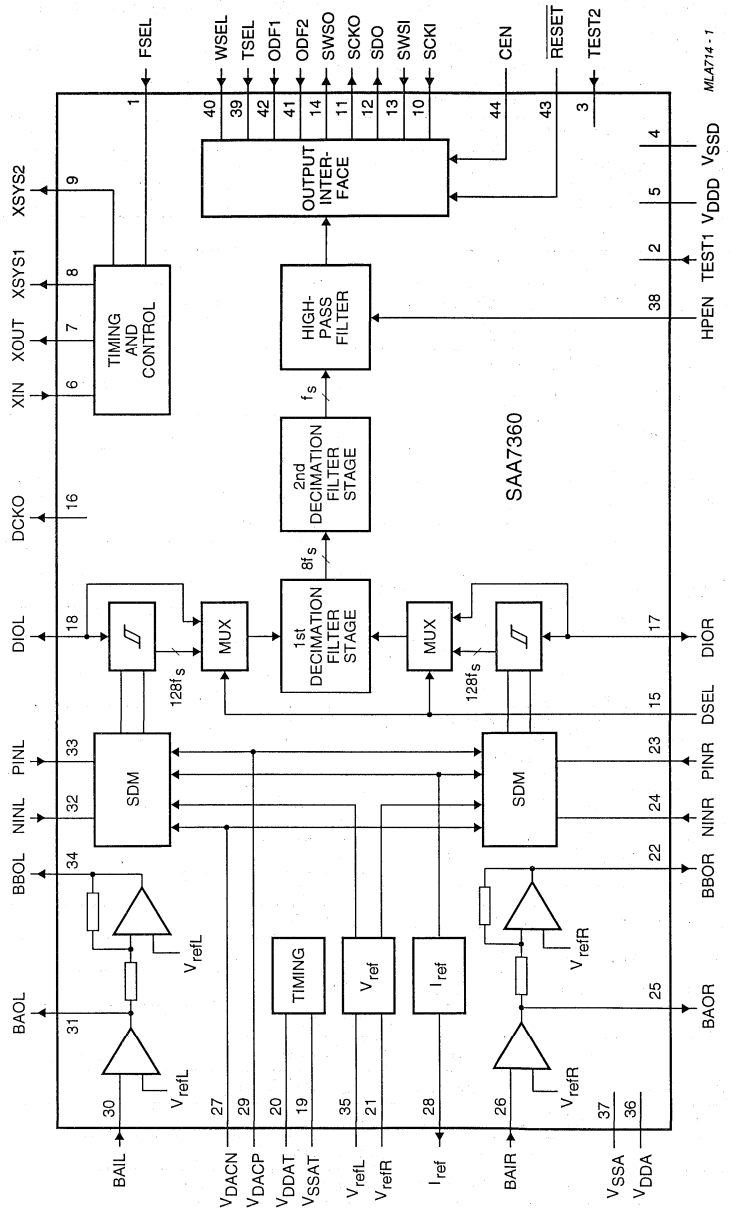


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSEL	1	Crystal frequency select input. This pin is used to select the master crystal frequency as follows: FSEL = HIGH = $256f_s$; FSEL = LOW = $512f_s$; if unconnected the pin will default HIGH.
TEST1	2	test input 1; this pin should be left open-circuit
TEST2	3	test input 2; this pin should be left open-circuit
V_{SSD}	4	supply ground for the digital section
V_{DDD}	5	supply voltage for the digital section (+5 V)
XIN	6	crystal oscillator input
XOUT	7	crystal oscillator output
XSYS1	8	system clock output
XSYS2	9	output clock at a frequency half the system clock frequency
SCKI	10	serial interface clock input
SCKO	11	serial interface clock output
SDO	12	serial interface data output
SWSI	13	serial interface word select input
SWSO	14	serial interface word select output
DSEL	15	input for selecting between the internally generated 1-bit code (DSEL = HIGH) or an externally generated 1-bit code (DSEL = LOW); if unconnected this pin defaults HIGH
DCKO	16	1-bit code clock output
DIOR	17	1-bit code input/output (right channel)
DIOL	18	1-bit code input/output (left channel)
V_{SSAT}	19	supply ground for the analog timing section
V_{DDAT}	20	supply voltage for the analog timing section (+5 V)
V_{refR}	21	voltage reference generator for the right channel analog section
BBOR	22	output of right channel buffer operational amplifier 'B'
PINR	23	positive input to right channel Sigma-Delta modulator
NINR	24	negative input to right channel Sigma-Delta modulator
BAOR	25	output of right channel buffer operational amplifier 'A'
BAIR	26	input of right channel buffer operational amplifier 'A'
V_{DACN}	27	negative voltage reference level input for the DACs
I_{ref}	28	current reference output
V_{DACP}	29	positive voltage reference level input for the DACs
BAIL	30	input of left channel buffer operational amplifier 'A'
BAOL	31	output of left channel buffer operational amplifier 'A'
NINL	32	negative input to left channel Sigma-Delta modulator
PINL	33	positive input to left channel Sigma-Delta modulator
BBOL	34	output of left channel buffer operational amplifier 'B'
V_{refL}	35	voltage reference generator for the left channel analog section
V_{DDA}	36	supply voltage for the analog section (+5 V)
V_{SSA}	37	supply ground for the analog section

SYMBOL	PIN	DESCRIPTION
HPEN	38	high-pass filter enable input (HPEN = HIGH = enabled); if unconnected this pin defaults HIGH
TSEL	39	input to select master (TSEL = LOW) or slave (TSEL = HIGH) operation of the serial interface; if unconnected this pin defaults HIGH
WSEL	40	input to indicate 16-bit (WSEL = HIGH) or 18-bit (WSEL = LOW) output data word length of the serial interface; if unconnected this pin defaults HIGH
ODF2 and ODF1	41 and 42	serial interface format inputs; these 2 pins determine the interface format in which the device will operate (see Chapter "Functional Description"); if unconnected these pins will default HIGH (I^2S format)
$\overline{\text{RESET}}$	43	Power-On Reset (POR) input (active LOW) to mute the digital output during power on
CEN	44	Chip enable input; this pin, when LOW, disables the operation of the device and 3-states the outputs of the serial interface bus. This enables the connection of one of more devices to the output bus; if unconnected this pin defaults HIGH.

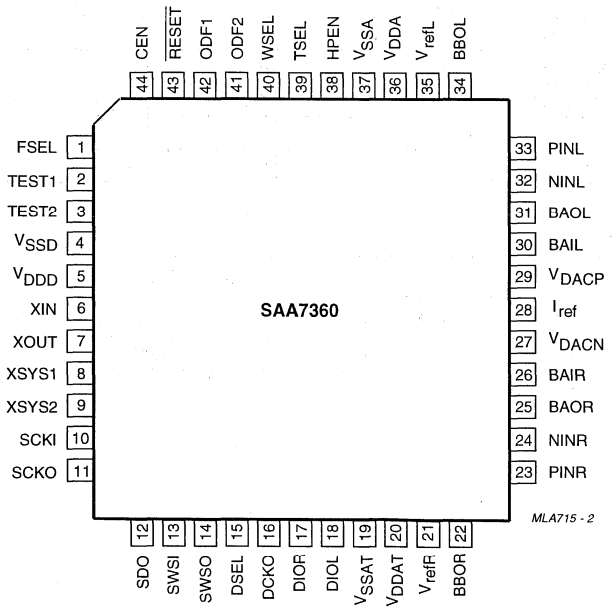


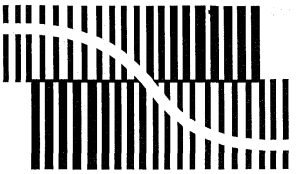
Fig.2 Pin configuration.

Bitstream conversion ADC for digital audio systems

SAA7366

FEATURES

- Integrated buffers for simple interfacing to analog inputs
- 4 flexible serial interface modes
- Overload detection of digital signal ≥–1 dB amplitude
- Selectable high-pass filter
- 18-bit serial output
- 3.4 to 5.5 V operation of digital part
- Standby mode
- SO24 package
- Small non-critical PCB layout.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7366 is a CMOS cost effective stereo analog-to-digital converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for digital acquisition of analog audio signals for digital audio systems such as:

- CD-recordable
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	4.5	5.0	5.5	V
f_i	clock input frequency	4.608	12.288	13.568	MHz
THD + N	total harmonic distortion + noise	–	–	–80	dB
DR	dynamic range	90	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7366T	24	SO24L	plastic	SOT137A

BLOCK DIAGRAM

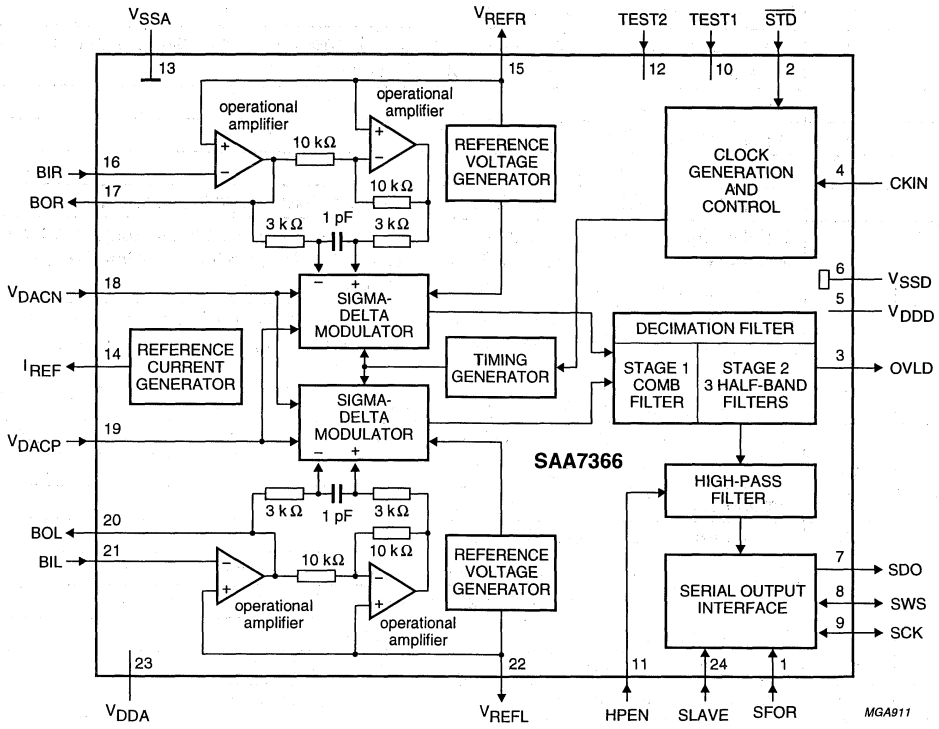


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	Serial interface output format select. Output format is selected as follows: SFOR HIGH = Format 1; SFOR LOW = Format 2.
$\overline{STD}$	2	Standby mode input (active LOW).
OVLD	3	Overload indication output. This pin indicates whether the internal digital signal is within 1 dB of maximum. In standby mode this output is high impedance.
CKIN	4	System clock input.
V_{DDD}	5	Supply for the digital section (3.4 to 5.5 V).
V_{SSD}	6	Ground supply for the digital section.
SDO	7	Serial interface data output. In standby mode this output is high impedance.
SWS	8	Serial interface word select signal. In master mode this pin outputs the serial interface word select signal. In slave mode this pin is the word select input to the serial interface. In standby mode this pin is always an input (high impedance).
SCK	9	Serial interface clock. In master mode this pin outputs the serial interface bit clock. In slave mode this pin is the input for the external bit clock. In standby mode this output is high impedance.
TEST1	10	Test input 1. This pin should be left open-circuit.
HPEN	11	High-pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH.
TEST2	12	Test input 2. This pin should be left open-circuit.
V_{SSA}	13	Ground supply for the analog section.
I_{REF}	14	Current reference output node.
V_{REFR}	15	$\frac{1}{2}V_{DDA}$ reference generator output for the right channel analog section.
BIR	16	Buffer operational amplifier inverting input for right channel.
BOR	17	Buffer operational amplifier output for right channel.
V_{DACN}	18	Negative 1-bit DAC reference voltage input, connected to 0 V.
V_{DACP}	19	Positive 1-bit DAC reference voltage input, connected to +5 V.
BOL	20	Buffer operational amplifier output for left channel.
BIL	21	Buffer operational amplifier inverting input for left channel.
V_{REFL}	22	$\frac{1}{2}V_{DDA}$ reference generator output for the left channel analog section.
V_{DDA}	23	Supply for the analog section.
SLAVE	24	Serial interface operating output mode master/slave select as follows: HIGH = slave mode; LOW = master mode. If unconnected the pin will default LOW.

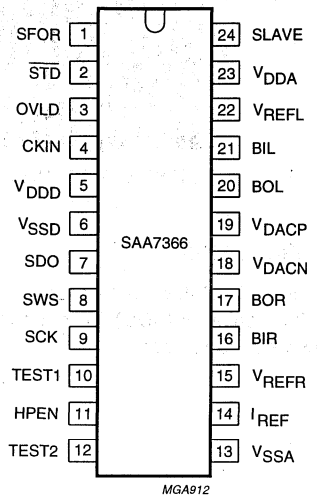


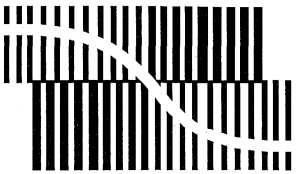
Fig.2 Pin configuration.

Bitstream conversion ADC for digital audio systems

SAA7367

FEATURES

- Total Harmonic Distortion plus Noise (THD + N) = –88 dB (0.004%); DR = 93 dB; S/N = 97 dB
- Simple interfacing to analog inputs
- Small, non-critical PCB layout
- Low pin-out SO24 package (pin-compatible to SAA7366)
- 4 flexible serial interface modes
- 4.5 to 5.5 V operation
- Standby mode
- Detection of digital signal ≥–1 dB amplitude
- Up to 18 significant bits serial output
- Selectable high-pass filter.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The SAA7367 is a CMOS low-cost stereo Analog-to-Digital Converter (ADC) using the Philips bitstream conversion technique.

APPLICATIONS

The device is designed for the digital acquisition of analog audio signals for digital audio systems such as:

- Compact Disc-Recordable (CD-R)
- Digital Compact Cassette (DCC)
- Digital Audio Tape (DAT).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	17	–	mA
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	13	–	mA
f_{BCK}	clock input frequency		4.60	12.288	12.8	MHz
f_s	sample rate		18	48	50	kHz
THD + N	total harmonic distortion plus noise	at 0 dB input	–	–88	–80	dB
DR	dynamic range	at –60 dB	90	93	–	dB
S/N	signal-to-noise ratio		–	97	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7367	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

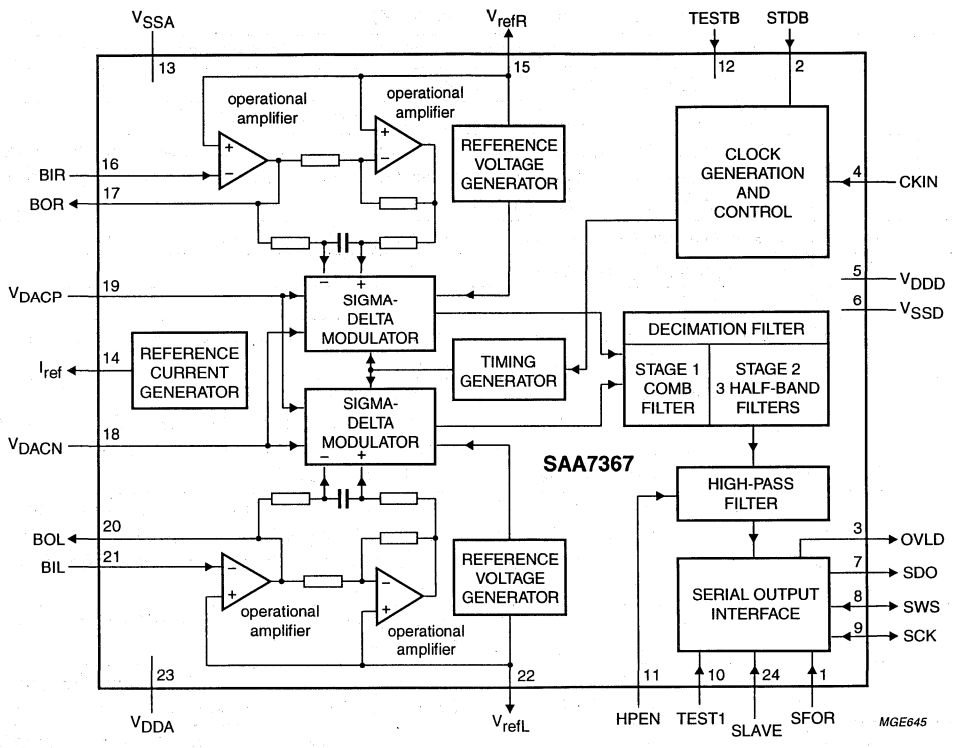


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SFOR	1	TTL level input; in normal mode this input selects the serial interface output format; output format is selected as follows: SFOR = HIGH selects Format 1 SFOR = LOW selects Format 2 (similar to I^2S)
STDB	2	schmitt-trigger input; in normal mode, this input is used to select standby mode:
		STDB = HIGH selects normal operation
		STDB = LOW selects standby mode (low power consumption)
OVLD	3	TTL level output; in normal mode this output indicates whether the internal digital signal is within 1 dB of maximum; if so, the output will go HIGH for 131072 clock cycles (approximately 11 ms); in standby mode this output is forced LOW
CKIN	4	CMOS level input; system clock input; nominally clocked at $256f_s$
V_{DDD}	5	digital supply voltage (4.5 to 5.5 V)
V_{SSD}	6	digital ground
SDO	7	TTL level output (3-state); in normal mode this pin outputs data from the serial interface; in standby mode, this output is high impedance
SWS	8	TTL level input/output; serial interface word select signal; in master mode (SLAVE = LOW), this pin outputs the serial interface word select signal; in slave mode (SLAVE = HIGH), this pin is the word select input to the serial interface; in standby mode (STDB = LOW) this pin is always an input (high impedance); for polarity: see Table 1
SCK	9	TTL level input/output; in master mode (SLAVE = LOW) the pin outputs the serial interface bit clock; in slave mode (SLAVE = HIGH) this pin is the input for the external bit clock; data on SDO is clocked out on the HIGH-to-LOW transition of SCK; the data is valid on the LOW-to-HIGH transition
TEST1	10	Test 1; TTL level input with internal pull-down; in slave mode (slave = HIGH), this pin is used to select extra serial interface formats (see Table 2)
HPEN	11	TTL level input; this input is used to enable the internal high-pass filter when HIGH; in scan-test mode (TESTB = LOW and TEST1 = LOW) this pin functions as 'scan chain c' input
TESTB	12	Test B; CMOS level input with internal pull-up; in normal applications, this input should be left HIGH
V_{SSA}	13	analog ground; this pin is internally connected to V_{SS} via the on-chip substrate contacts
I_{ref}	14	current reference generator output; 33 kΩ in parallel with 22 nF is connected from this pin to V_{SSA}
V_{refR}	15	right channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
BIR	16	buffer operational amplifier inverting input for right channel
BOR	17	buffer operational amplifier output for right channel
V_{DACN}	18	negative 1-bit DAC reference voltage input, connected to 0 V
V_{DACP}	19	positive 1-bit DAC reference voltage input, connected to +5 V
BOL	20	buffer operational amplifier output for left channel
BIL	21	buffer operational amplifier inverting input for left channel
V_{refL}	22	left channel analog reference output voltage ($\frac{1}{2}V_{DDA}$)
V_{DDA}	23	analog supply voltage (4.5 to 5.5 V)

SYMBOL	PIN	DESCRIPTION
SLAVE	24	TTL level input; used to select the serial interface operating mode: SLAVE = HIGH selects slave mode SLAVE = LOW selects master mode

Table 1 SWS polarity

CONDITIONS			POLARITY
SLAVE AND TEST1	SWS	SFOR	
SLAVE = LOW or TEST1 = LOW	LOW	LOW	left data
	LOW	HIGH	right data
SLAVE = HIGH and TEST1 = HIGH	LOW	LOW	right data
	LOW	HIGH	left data

Table 2 Selection of serial interface formats via TEST1

CONDITIONS		SELECTED FORMAT
SFOR	TEST1	
HIGH	LOW	format 1
	HIGH	format 2
LOW	LOW	format 3
	HIGH	format 4

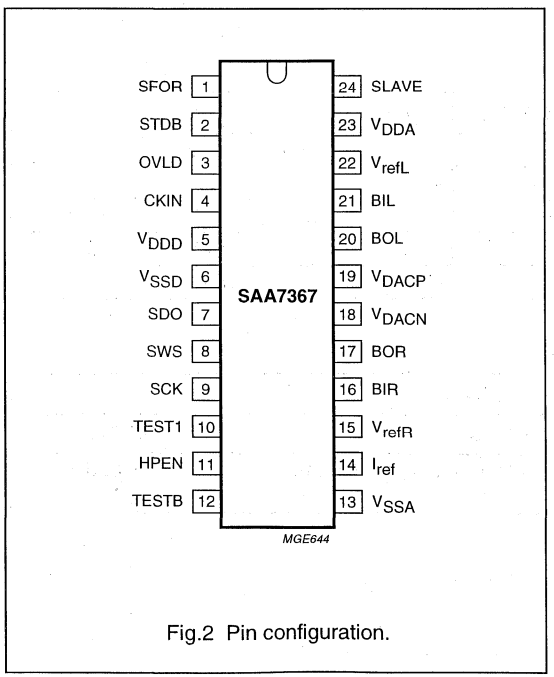


Fig.2 Pin configuration.

Digital servo processor and Compact Disc decoder (CD7)

SAA7370

1 FEATURES

- CD ROM mode
- Up to 4 times-speed mode
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Up to 80 kHz jump performance
- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7370 (CD7) is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7370	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

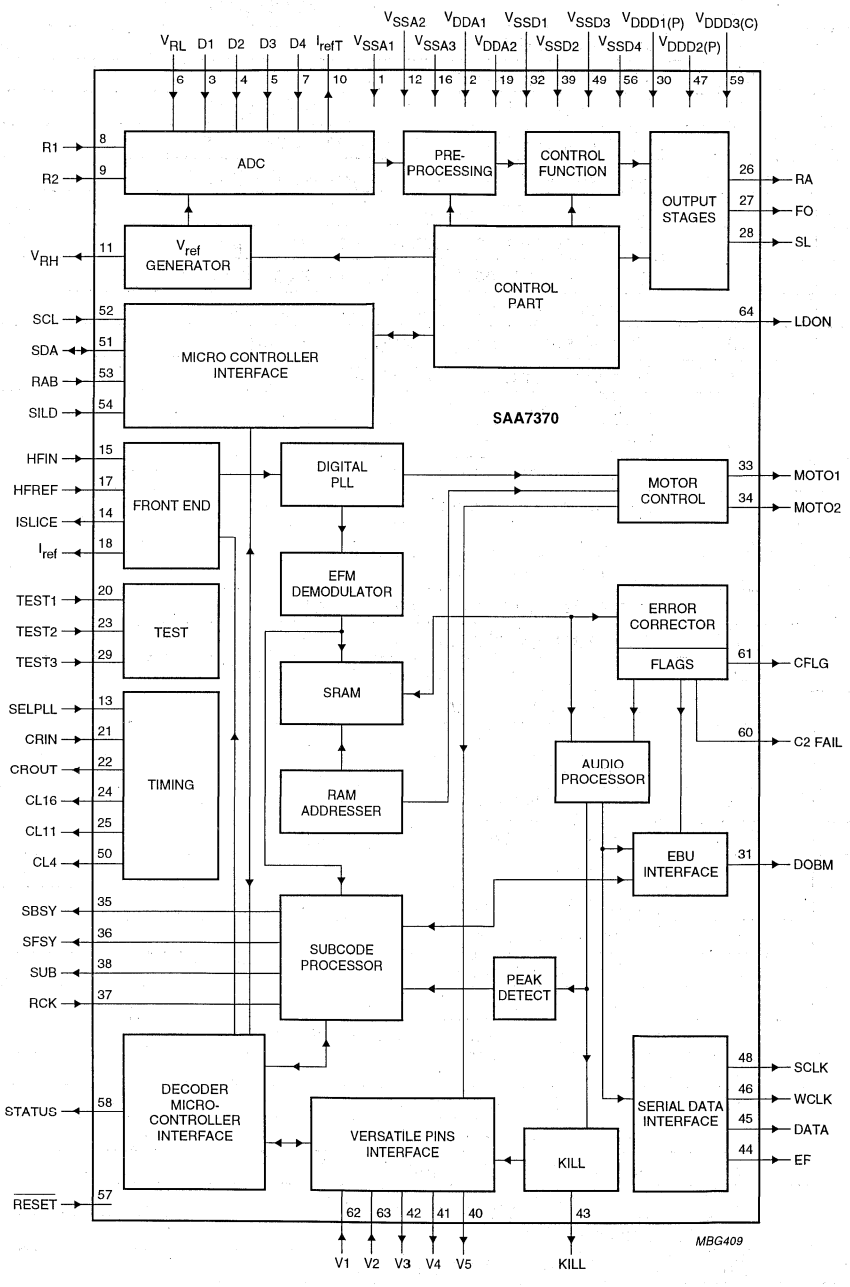


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448 MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

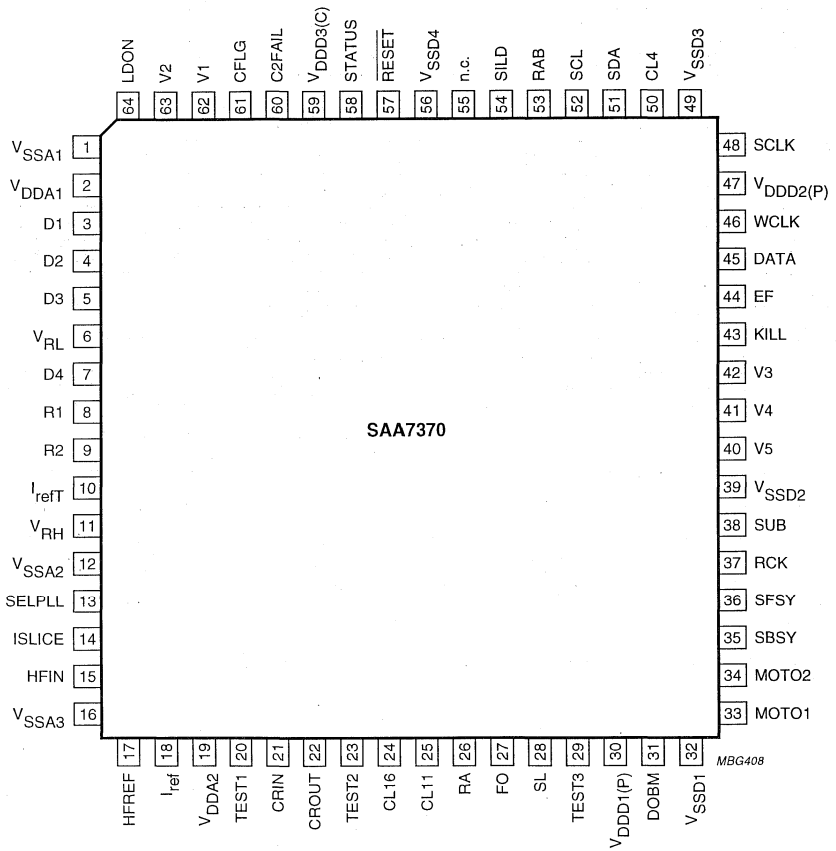


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Decoder part

7.1.1 PRINCIPLE OPERATIONAL MODES OF THE DECODER

The decoding part can operate at different disc speeds, from single-speed (n = 1) up to 4 times speed (n = 4). The factor 'n' is called the overspeed factor. A simplified data flow through the decoder part is illustrated in Fig.6.

7.1.2 DECODING SPEED AND CRYSTAL FREQUENCY

The SAA7370 is a multi-speed decoding device, with an internal phase-locked loop (PLL) clock multiplier. Depending on the crystal frequency used and the internal clock settings (selectable via registers B and E), the playback speeds shown in Table 1 are possible, where 'n' is the overspeed factor. An internal clock multiplier is present, controlled by SELPLL, and should only be used if an 8.4672 MHz crystal, ceramic resonator or external clock is present.

7.1.3 LOCK-TO-DISC MODE

For high speed CD ROM applications, the SAA7370 has a special mode, the lock-to-disc mode. This allows Constant Angular Velocity (CAV) disc playback with varying input data rates from the inside-to-outside of the disc. In the lock-to-disc mode, the FIFO is blocked and the decoder will adjust its output data rate to the disc speed. Hence, the frequency of the I²S-bus (WCLK and SCLK) clocks are dependent on the disc speed. In the lock-to-disc mode there is a limit on the maximum variation in disc speed that the SAA7370 will follow. Disc speeds must always be within 25% to 100% range of their nominal value. The lock-to-disc mode is enabled/disabled by register E.

7.1.4 STANDBY MODES

The SAA7370 may be placed in two standby modes selected by register B (it should be noted that the device core is still active):

Standby 1: 'CD-STOP' mode. Most I/O functions are switched off.

Standby 2: 'CD-PAUSE' mode. Audio output features are switched off, but the motor loop, the motor output and the subcode interfaces remain active. This is also called a 'Hot Pause'.

In the standby modes the various pins will have the following values:

MOTO1 and MOTO2: put in high-impedance, PWM mode (standby 1 and reset, operating in standby 2). Put in high-impedance, PDM mode (standby 1 and reset, operating in standby 2).

SCL, SDA, SILD and RAB: no interaction. Normal operation continues.

SCLK, WCLK, DATA, EF, CL11 and DOBM: 3-state in both standby modes. Normal operation continues after reset.

CRIN, CROUT, CL16 and CL4: no interaction. Normal operation continues.

V1, V2, V3, V4, V5, CFLG and C2FAIL: no interaction. Normal operation continues.

Table 1 Playback speeds

REGISTER B	REGISTER E	SELPLL	CRYSTAL FREQUENCY (MHz)			CL11 FREQUENCY (MHz)[1]
			33.8688	16.9344	8.4672	
00xx	0xxx	0	n = 1	–	–	11.2896
00xx	0xxx	1	–	–	n = 1	11.2896
01xx	0xxx	0	–	n = 1	–	5.6448
10xx	0xxx	0	n = 2	–	–	11.2896
10xx	0xxx	1	–	–	n = 2	11.2896
11xx	0xxx	0	–	n = 2[2]	–	5.6448
00xx	1xxx	0	n = 4[2]	–	–	11.2896
00xx	1xxx	1	–	–	n = 4	11.2896
01xx	1xxx	0	–	n = 4[2]	–	5.6448

Note

1. The CL11 output is always a 5.6448 MHz clock if a 16.9344 MHz external clock is used and SELPLL = 0.
2. Data capture performance is not optimized for these options.

1 FEATURES

- CD-ROM mode
- Up to 8 times-speed mode
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support
- Up to 80 kHz (8.4672 MHz crystal) or 16 MHz (16.9344 MHz crystal) jump performance
- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High level servo control option
- High level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal for up to 4 times speed mode or 16.9344 MHz crystal for up to 8 times-speed mode.

2 GENERAL DESCRIPTION

The SAA7370A (CD7) is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7370A	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

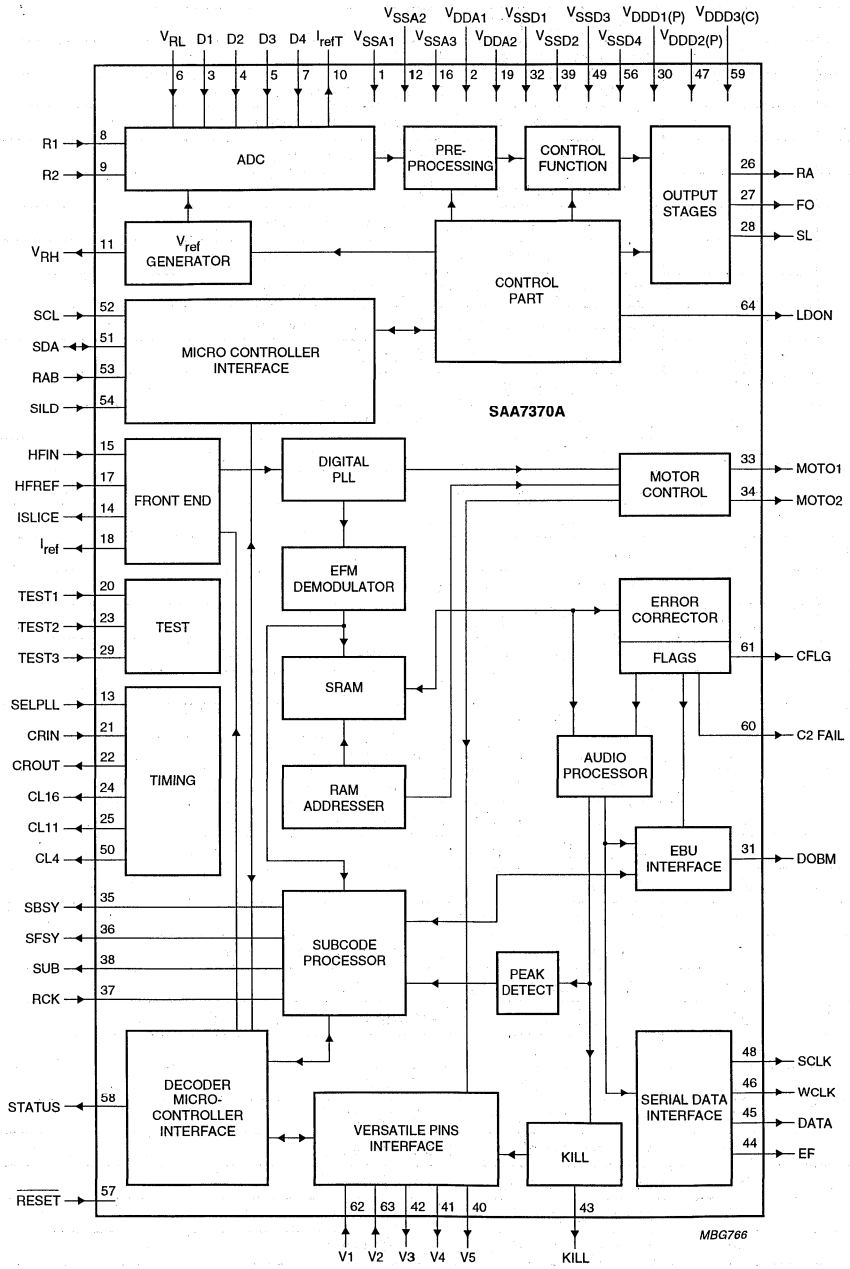


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz (or 33.8688 MHz) system clock output
CL11	25	11.2896 or 5.6448 MHz (or 22.5792 MHz) clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47(1)	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49(1)	digital ground 3
CL4	50	4.2336 MHz (or 8.4672 MHz) microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56(1)	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59(1)	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

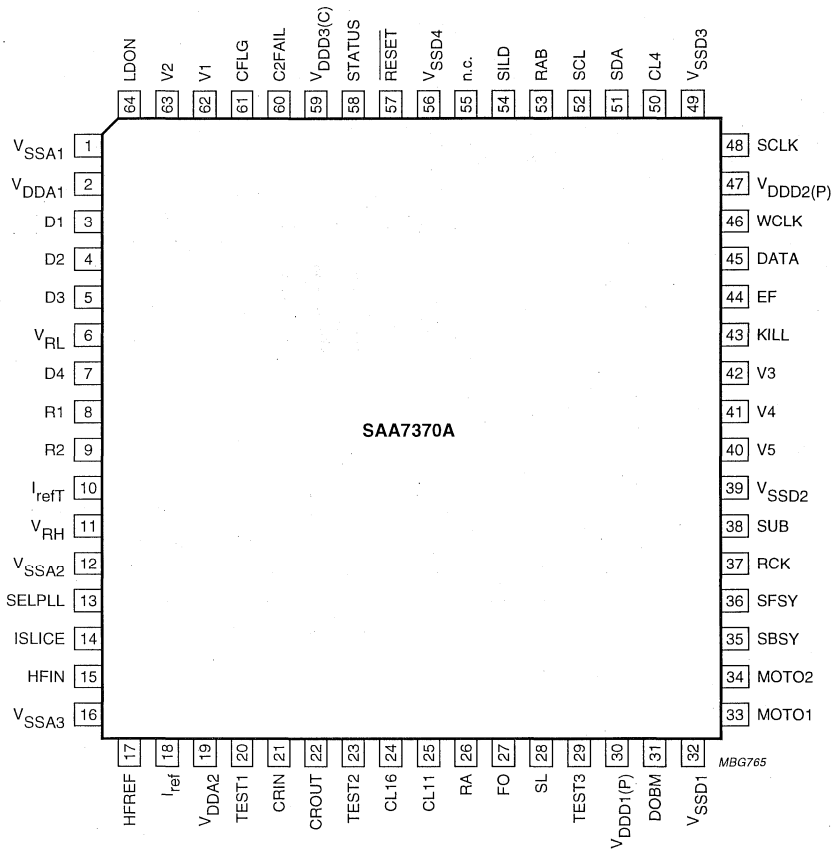


Fig.2 Pin configuration.

Single-chip digital servo processor and Compact Disc decoder (CD7)

SAA7372

1 FEATURES

- CD ROM mode
- Single and double-speed modes
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7372 is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7372	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

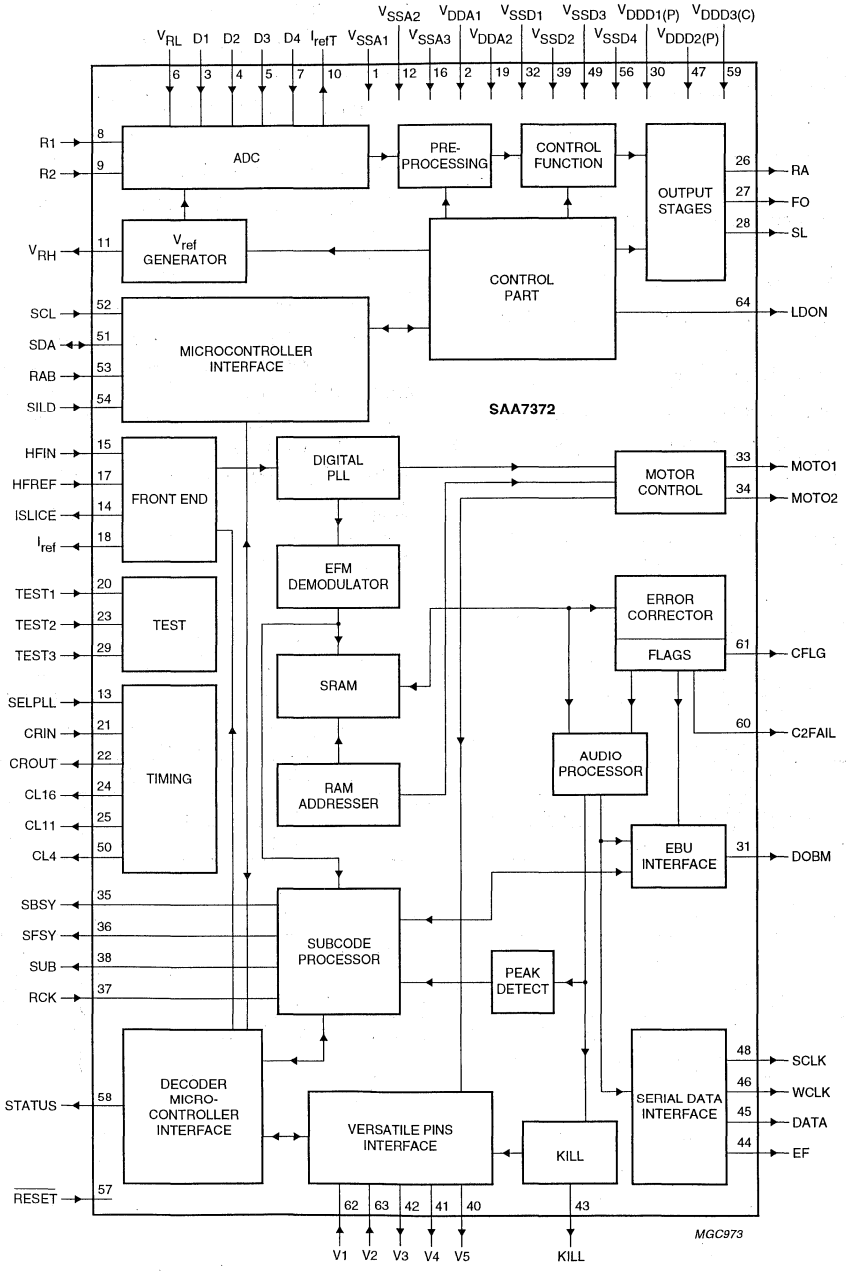


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448 MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode output bits (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes and $1f_s$ modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

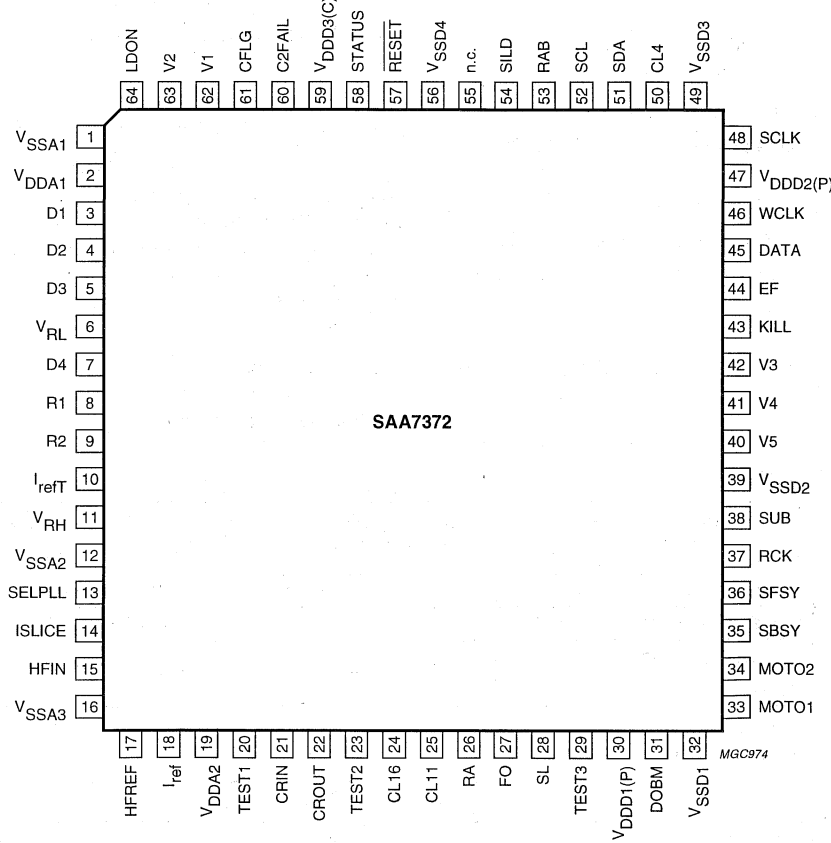


Fig.2 Pin configuration.

Low voltage digital servo processor and Compact Disc decoder (CD7LV)

SAA7374

1 FEATURES

- CD-ROM mode
- Single and double-speed modes
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7374 (CD7LV) is a low-voltage chip which combines the functions of a CD decoder IC and Digital Servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated. Extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	3.3	3.6	V
I_{DD}	supply current	n = 1 mode	–	28	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7374	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

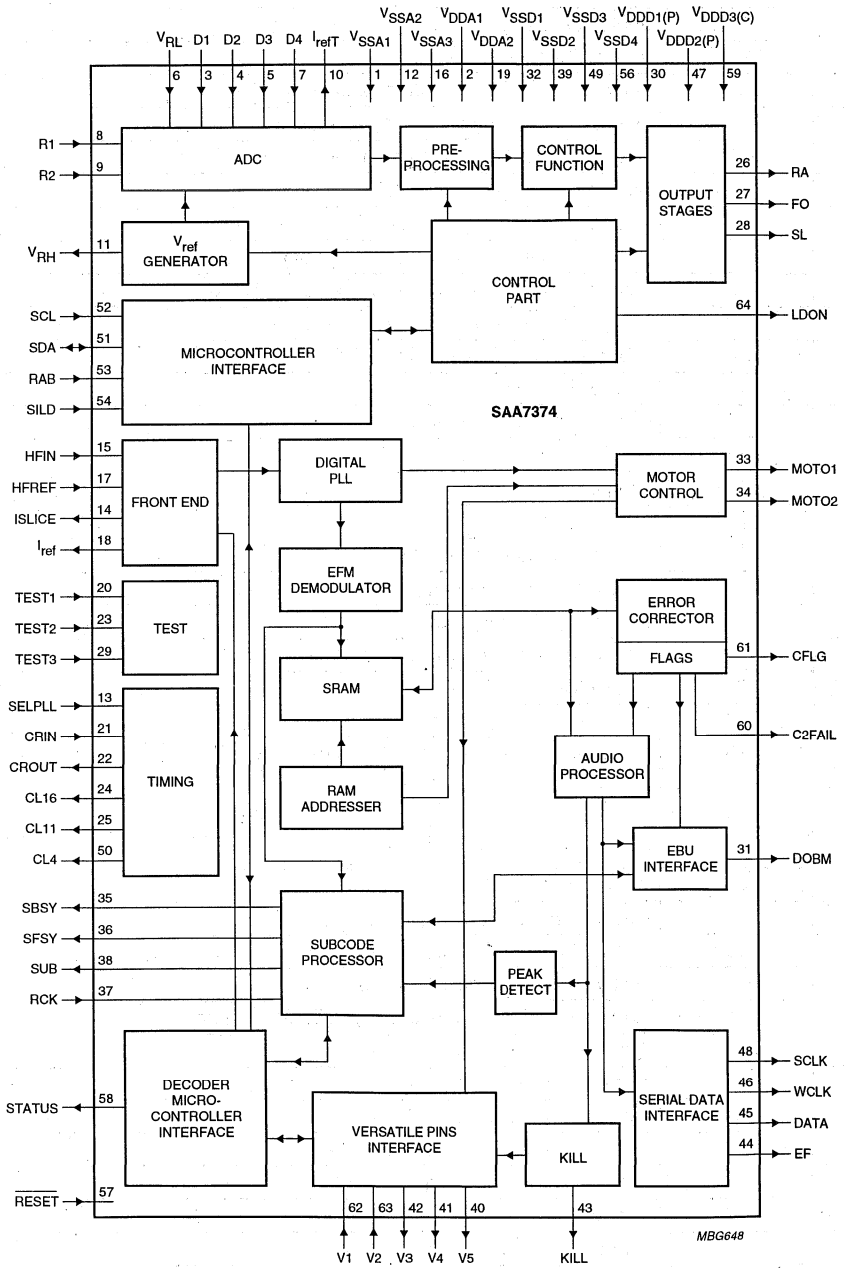


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM and $1f_s$ modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

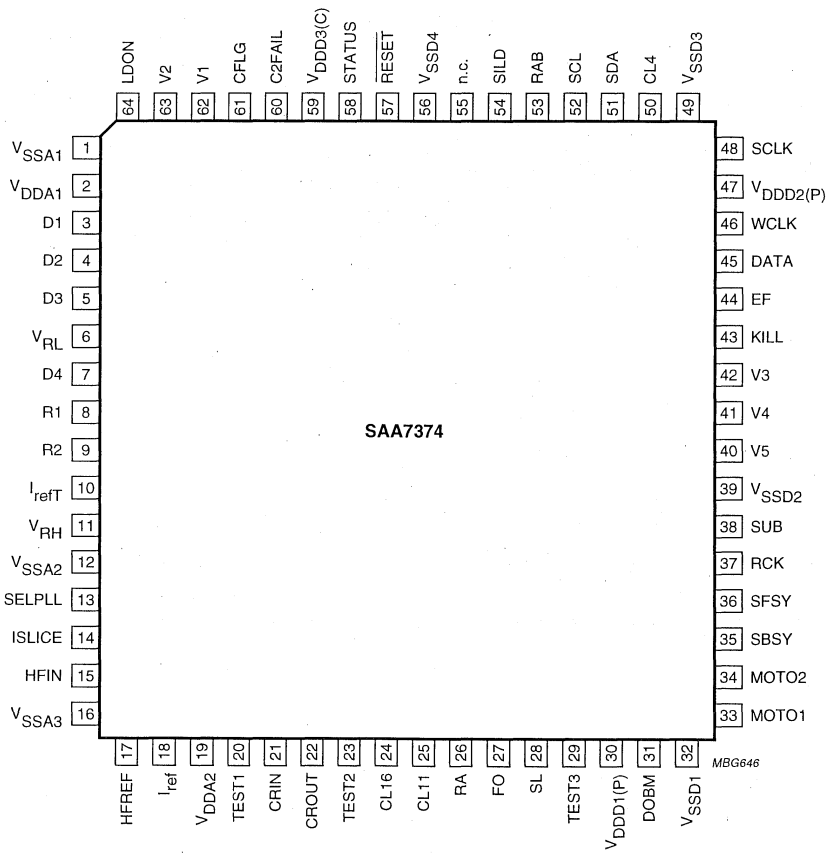


Fig.2 Pin configuration.

Digital servo processor and Compact Disc decoder (CD7) SAA7376

1 FEATURES

- Single-speed mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio only
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high-level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed loop gain control available for focus and radial loops
- Pulsed sledge support
- Microcontroller loading LOW
- High-level servo control option
- High-level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I^2C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal.

2 GENERAL DESCRIPTION

The SAA7376 is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

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3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current		–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		−10	–	+70	°C
T_{stg}	storage temperature		−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7376	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5 BLOCK DIAGRAM

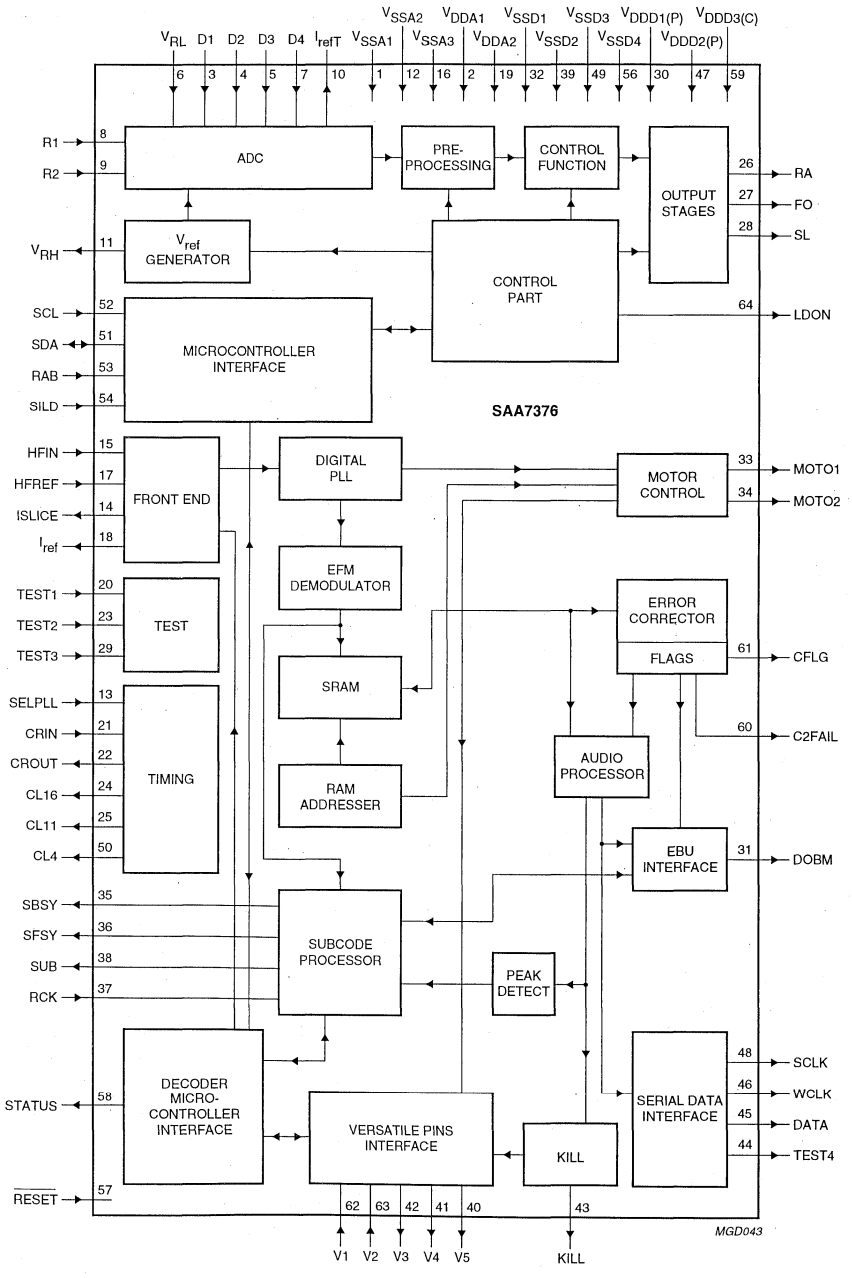

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz system clock output
CL11	25	11.2896 or 5.6448 MHz clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode output bits (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
TEST4	44	test output pin; this pin should be left unconnected
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47(1)	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49(1)	digital ground 3
CL4	50	4.2336 MHz microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56(1)	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59(1)	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

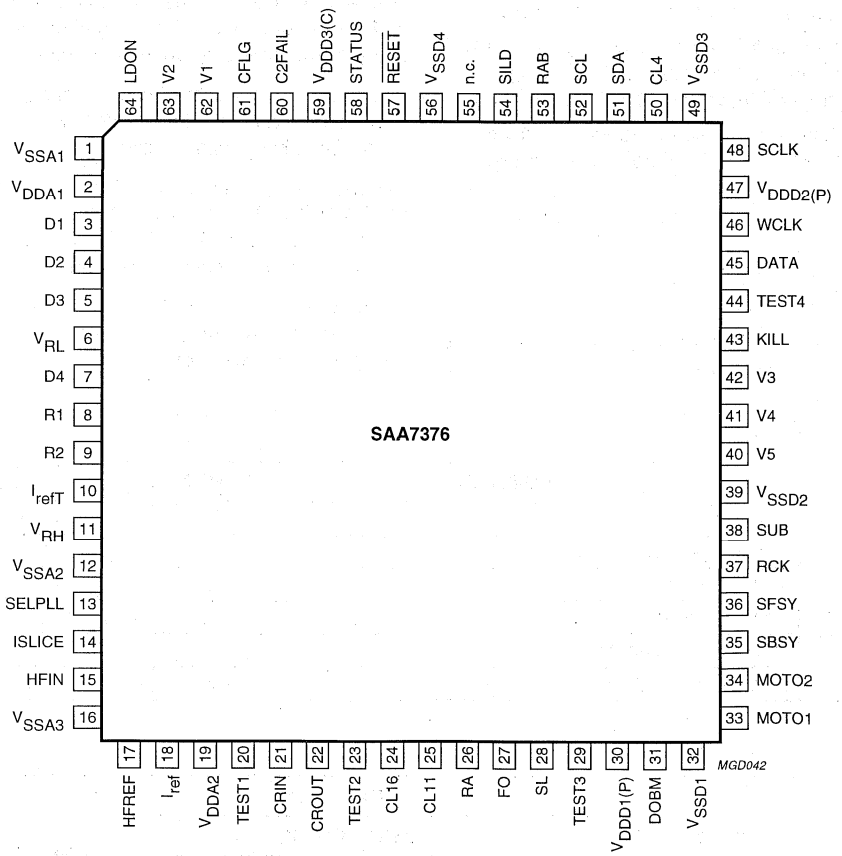

Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (ELM)

SAA7380

1 FEATURES

- CD-ROM (Mode 1) and CD-I (Mode 2 - Form 1 and Form 2) formats supported
- Real-time error detection and correction in hardware
- Suitable for 6 × speed, n = 6
- Maximum host transfer burst rate of 11.1 Mbyte/s
- Corrects two errors per symbol with erasure correction
- 36 kbit of on-chip error correction buffer RAM
- 12-byte command FIFO and 12-byte status FIFO
- Compatible with the Advanced Technology Attachment (ATA) register set and the Advanced Technology Attachment Program Interface (ATAPI) command set
- Operates with popular memories. (up to 128 kbyte SRAM; 1 to 16 Mbit DRAM, different speed grades, nibble or byte wide)
- Interface to Integrated Drive Electronics (IDE) bus without external bus drivers
- Q-to-W subcode buffering, de-interleaving and correction are supported
- Device can operate with audio RAMs. A RAM test allows bad segments to be identified.

2 GENERAL DESCRIPTION

The SAA7380 decoder is a block decoder buffer manager for high-speed CD-ROM applications that integrates real-time error correction and detection and host interface data transfer functions into a single chip.

The SAA7380 has an on-chip 36-kbit memory. This memory is used as a buffer memory for error and erasure corrections. The chip also has a buffer memory interface thus enabling the connection of SRAM up to 128 kbytes, or DRAM up to 16 Mbits. The on-chip memory is sufficient to buffer 1 sector of data. The external memory can buffer many more, depending on memory size.

The error corrector of the SAA7380 can perform 2-pass error correction in real-time. Buffer memory for this correction is integrated on-chip.

The SAA7380 has an host interface that is compatible with the SANYO LC89510 or OAK OTI-012 and also compatible with the ATA/IDE/ATAPI hard disc interface bus. (All ATAPI registers are present in hardware).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	4.5	5	5.5	V
I_{DDD}	supply current	–	60	–	mA
f_{clk}	clock frequency	15.2	33.8688	35	MHz
T_{amb}	operating ambient temperature	0	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7380GP	QFP80	plastic quad flat package; 80 leads; lead length 1.95 mm; body 14 × 20 × 2.8 mm	SOT318-2

5 BLOCK DIAGRAM

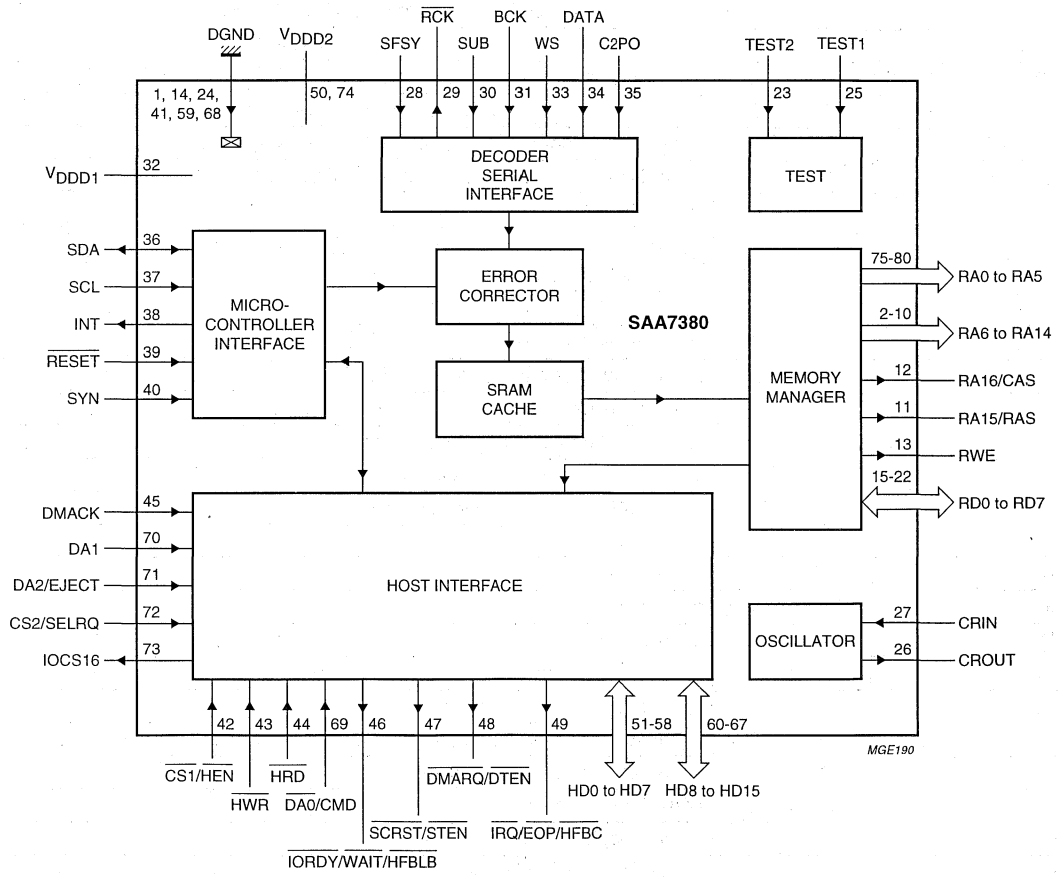

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DGND1	1	–	digital ground 1
RA6	2	O	buffer RAM address bus output line 6
RA7	3	O	buffer RAM address bus output line 7
RA8	4	O	buffer RAM address bus output line 8
RA9	5	O	buffer RAM address bus output line 9
RA10	6	O	buffer RAM address bus output line 10
RA11	7	O	buffer RAM address bus output line 11 (SRAM) only
RA12	8	O	buffer RAM address bus output line 12 (SRAM) only
RA13	9	O	buffer RAM address bus output line 13 (SRAM) only
RA14	10	O	buffer RAM address bus output line 14 (SRAM) only
RA15/RAS	11	O	buffer RAM address bus output line 15 (SRAM) or RAS (DRAM)
RA16/CAS	12	O	buffer RAM address bus output line 16 (SRAM) or CAS (DRAM)
RWE	13	O	buffer RAM write enable output
DGND2	14	–	digital ground 2
RD0	15	I/O	buffer RAM data bus bidirectional line 0
RD1	16	I/O	buffer RAM data bus bidirectional line 1
RD2	17	I/O	buffer RAM data bus bidirectional line 2
RD3	18	I/O	buffer RAM data bus bidirectional line 3
RD4	19	I/O	buffer RAM data bus bidirectional line 4
RD5	20	I/O	buffer RAM data bus bidirectional line 5
RD6	21	I/O	buffer RAM data bus bidirectional line 6
RD7	22	I/O	buffer RAM data bus bidirectional line 7
TEST2	23	I	test input 2
DGND3	24	–	digital ground 3
TEST1	25	I	test input 1
CROUT	26	O	clock oscillator output
CRIN	27	I	clock oscillator input
SFSY	28	I	serial subcode input frame sync input
$\overline{\text{RCK}}$	29	O	serial subcode clock output (active LOW)
SUB	30	I	serial input for Q-to-W subcode input
BCK	31	I	serial interface bit clock input
V_{DDD1}	32	–	digital supply voltage 1 (3.3 V)
WS	33	I	serial interface word clock input
DATA	34	I	serial data input
C2PO	35	I	serial interface flag input
SDA	36	I/O	sub-CPU serial data input/output
SCL	37	I	sub-CPU serial clock input
INT	38	O	sub-CPU open-collector interrupt output
$\overline{\text{RESET}}$	39	I	power-on reset input (active LOW)
SYN	40	I	sync signal input from sub-CPU

SYMBOL	PIN	I/O	DESCRIPTION
DGND4	41	–	digital ground 4
$\overline{CS1}/\overline{HEN}$	42	I	host interface enable input (active LOW)
$\overline{HWR}$	43	I	host interface write enable input (active LOW)
$\overline{HRD}$	44	I	host interface read enable input (active LOW)
DMACK	45	I	DMA acknowledge input
$\overline{IORDY}/\overline{WAIT}/\overline{HFBLB}$	46	O	host interface wait output (active LOW); 3-state control
$\overline{SCRST}/\overline{STEN}$	47	O	host interface status enable output ATAPI sub-CPU reset signal (active LOW)
$\overline{DMARQ}/\overline{DTEN}$	48	O	ATAPI DMA request host interface data enable output (active LOW); 3-state control
$\overline{IRQ}/\overline{EOP}/\overline{HFBC}$	49	O	host interface end of process flag output ATAPI host interrupt request (active LOW); 3-state control
V_{DDD2}	50	–	digital supply voltage 2 (5 V)
HD0	51	I/O	host interface data bus input/output line 0
HD1	52	I/O	host interface database input/output line 1
HD2	53	I/O	host interface database input/output line 2
HD3	54	I/O	host interface data bus input/output line 3
HD4	55	I/O	host interface data bus input/output line 4
HD5	56	I/O	host interface data bus input/output line 5
HD6	57	I/O	host interface data bus input/output line 6
HD7	58	I/O	host interface data bus input/output line 7
DGND5	59	–	digital ground 5
HD8	60	I/O	host interface data bus input/output line 8
HD9	61	I/O	host interface data bus input/output line 9
HD10	62	I/O	host interface data bus input/output line 10
HD11	63	I/O	host interface data bus input/output line 11
HD12	64	I/O	host interface data bus input/output line 12
HD13	65	I/O	host interface data bus input/output line 13
HD14	66	I/O	host interface data bus input/output line 14
HD15	67	I/O	host interface data bus input/output line 15
DGND6	68	–	digital ground 6
$\overline{DA0}$/CMD	69	I	host interface data input (active LOW)/command select input host interface address line 0
DA1	70	I	ATAPI address line input 1
DA2/EJECT	71	I	ATAPI address line input 2
CS2/SELRQ	72	I	ATAPI chip select input 2
IOCS16	73	O	ATAPI 16-bit data select output
V_{DDD2}	74	–	digital supply voltage 2 (5 V)
RA0	75	O	buffer RAM address bus output line 0
RA1	76	O	buffer RAM address bus output line 1
RA2	77	O	buffer RAM address bus output line 2

SYMBOL	PIN	I/O	DESCRIPTION
RA3	78	O	buffer RAM address bus output line 3
RA4	79	O	buffer RAM address bus output line 4
RA5	80	O	buffer RAM address bus output line 5

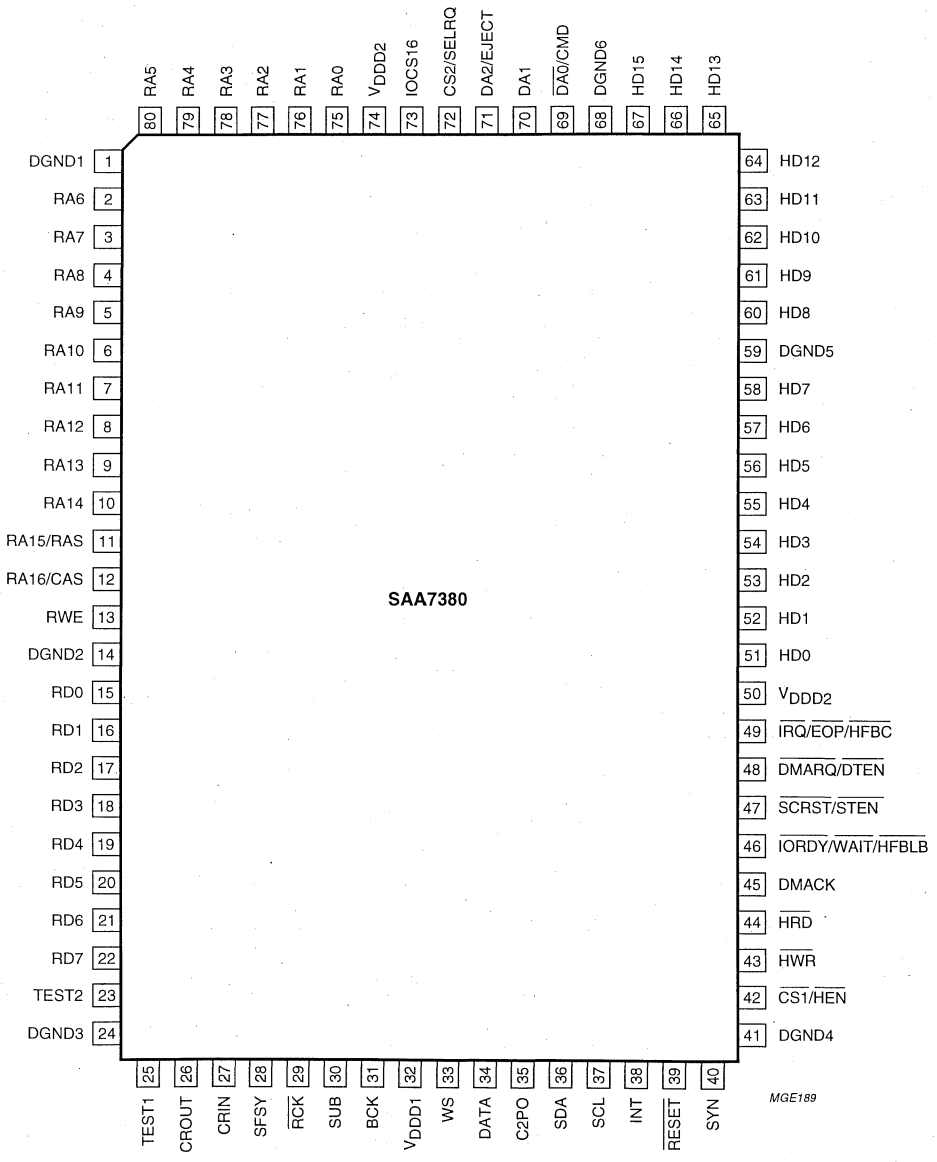

Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (ELM)

SAA7382

1 FEATURES

- CD-ROM (Mode 1) and CD-I (Mode 2 - Form 1 and Form 2) formats supported
- Real-time error detection and correction in hardware
- Suitable for double speed, n = 2.
- Maximum host transfer burst rate of 8.3 Mbyte/s
- Corrects two errors per symbol with erasure correction
- 36 kbit of on-chip error correction buffer RAM
- 12-byte command FIFO and 12-byte status FIFO
- Compatible with the Advanced Technology Attachment (ATA) register set and the Advanced Technology Attachment Program Interface (ATAPI) command set
- Operates with popular memories. (up to 128 kbyte SRAM; 1 to 16 Mbit DRAM, different speed grades, nibble or byte wide)
- Interface to Integrated Drive Electronics (IDE) bus without external bus drivers
- Q-to-W subcode buffering, de-interleaving and correction are supported
- Device can operate with audio RAMs. A RAM test allows bad segments to be identified.

2 GENERAL DESCRIPTION

The SAA7382 decoder is a block decoder buffer manager for high-speed CD-ROM applications that integrates real-time error correction and detection and host interface data transfer functions into a single chip.

The SAA7382 has an on-chip 36-kbit memory. This memory is used as a buffer memory for error and erasure corrections. The chip also has a buffer memory interface thus enabling the connection of SRAM up to 128 kbytes, or DRAM up to 16 Mbits. The on-chip memory is sufficient to buffer 1 sector of data. The external memory can buffer many more, depending on memory size.

The error corrector of the SAA7382 can perform 2-pass error correction in real-time. Buffer memory for this correction is integrated on-chip.

The SAA7382 has an host interface that is compatible with the SANYO LC89510 or OAK OTI-012 and also compatible with the ATA/IDE/ATAPI hard disc interface bus. (All ATAPI registers are present in hardware).

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3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	4.5	5	5.5	V
I_{DDD}	supply current	–	60	–	mA
f_{clk}	clock frequency	15.2	16.9344	18.0	MHz
T_{amb}	operating ambient temperature	0	–	+70	°C
T_{stg}	storage temperature	–55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7382GP	QFP80	plastic quad flat package; 80 leads; lead length 1.95 mm; body 14 × 20 × 2.8 mm	SOT318-2

5 BLOCK DIAGRAM

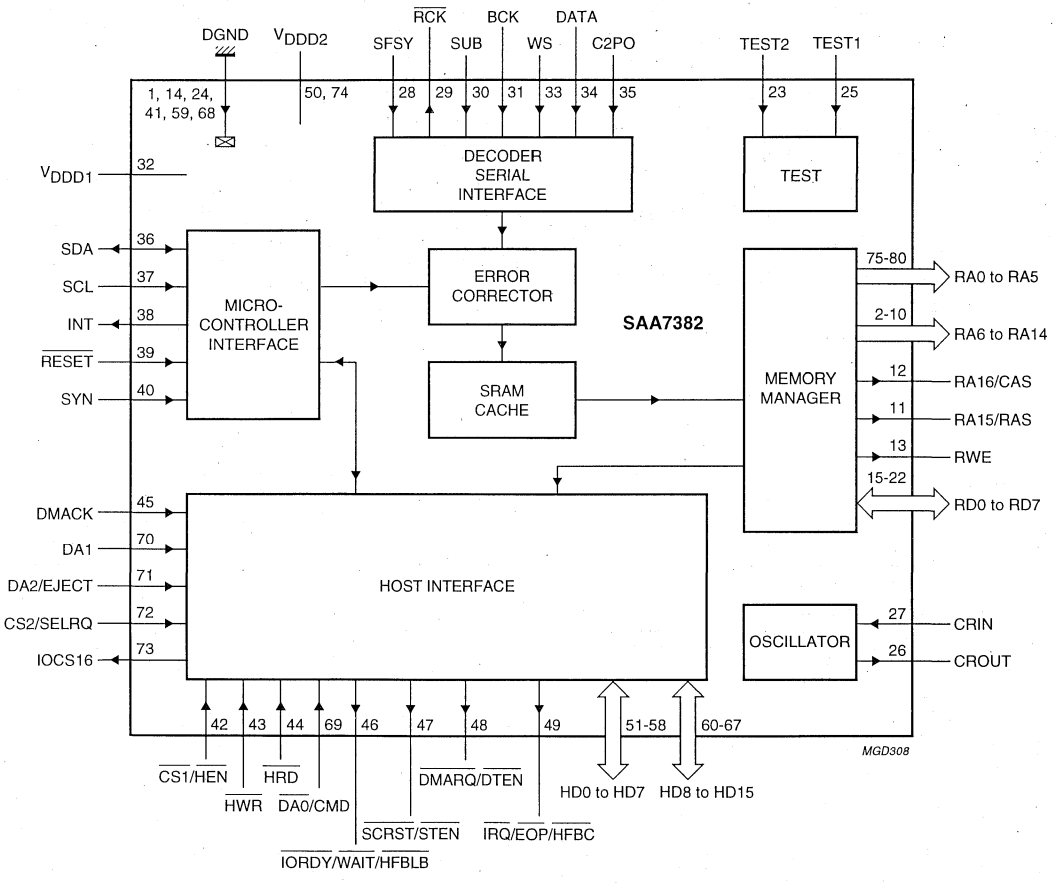


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DGND1	1	–	digital ground 1
RA6	2	O	buffer RAM address bus output line 6
RA7	3	O	buffer RAM address bus output line 7
RA8	4	O	buffer RAM address bus output line 8
RA9	5	O	buffer RAM address bus output line 9
RA10	6	O	buffer RAM address bus output line 10
RA11	7	O	buffer RAM address bus output line 11 (SRAM) only
RA12	8	O	buffer RAM address bus output line 12 (SRAM) only
RA13	9	O	buffer RAM address bus output line 13 (SRAM) only
RA14	10	O	buffer RAM address bus output line 14 (SRAM) only
RA15/RAS	11	O	buffer RAM address bus output line 15 (SRAM) or RAS (DRAM)
RA16/CAS	12	O	buffer RAM address bus output line 16 (SRAM) or CAS (DRAM)
RWE	13	O	buffer RAM write enable output
DGND2	14	–	digital ground 2
RD0	15	I/O	buffer RAM data bus bidirectional line 0
RD1	16	I/O	buffer RAM data bus bidirectional line 1
RD2	17	I/O	buffer RAM data bus bidirectional line 2
RD3	18	I/O	buffer RAM data bus bidirectional line 3
RD4	19	I/O	buffer RAM data bus bidirectional line 4
RD5	20	I/O	buffer RAM data bus bidirectional line 5
RD6	21	I/O	buffer RAM data bus bidirectional line 6
RD7	22	I/O	buffer RAM data bus bidirectional line 7
TEST2	23	I	test input 2
DGND3	24	–	digital ground 3
TEST1	25	I	test input 1
CROUT	26	O	clock oscillator output
CRIN	27	I	clock oscillator input
SFSY	28	I	serial subcode input frame sync input
$\overline{\text{RCK}}$	29	O	serial subcode clock output (active LOW)
SUB	30	I	serial input for Q-to-W subcode input
BCK	31	I	serial interface bit clock input
V_{DDD1}	32	–	digital supply voltage 1 (3.3 V)
WS	33	I	serial interface word clock input
DATA	34	I	serial data input
C2PO	35	I	serial interface flag input
SDA	36	I/O	sub-CPU serial data input/output
SCL	37	I	sub-CPU serial clock input
INT	38	O	sub-CPU open-collector interrupt output
$\overline{\text{RESET}}$	39	I	power-on reset input (active LOW)
SYN	40	I	sync signal input from sub-CPU

SYMBOL	PIN	I/O	DESCRIPTION
DGND4	41	–	digital ground 4
$\overline{CS1}/\overline{HEN}$	42	I	host interface enable input (active LOW)
$\overline{HWR}$	43	I	host interface write enable input (active LOW)
$\overline{HRD}$	44	I	host interface read enable input (active LOW)
DMACK	45	I	DMA acknowledge input
$\overline{IORDY}/\overline{WAIT}/\overline{HFBLB}$	46	O	host interface wait output (active LOW); 3-state control
$\overline{SCRST}/\overline{STEN}$	47	O	host interface status enable output ATAPI sub-CPU reset signal (active LOW)
$\overline{DMARQ}/\overline{DTEN}$	48	O	ATAPI DMA request host interface data enable output (active LOW); 3-state control
$\overline{IRQ}/\overline{EOP}/\overline{HFBC}$	49	O	host interface end of process flag output ATAPI host interrupt request (active LOW); 3-state control
V_{DDD2}	50	–	digital supply voltage 2 (5 V)
HD0	51	I/O	host interface data bus input/output line 0
HD1	52	I/O	host interface database input/output line 1
HD2	53	I/O	host interface database input/output line 2
HD3	54	I/O	host interface data bus input/output line 3
HD4	55	I/O	host interface data bus input/output line 4
HD5	56	I/O	host interface data bus input/output line 5
HD6	57	I/O	host interface data bus input/output line 6
HD7	58	I/O	host interface data bus input/output line 7
DGND5	59	–	digital ground 5
HD8	60	I/O	host interface data bus input/output line 8
HD9	61	I/O	host interface data bus input/output line 9
HD10	62	I/O	host interface data bus input/output line 10
HD11	63	I/O	host interface data bus input/output line 11
HD12	64	I/O	host interface data bus input/output line 12
HD13	65	I/O	host interface data bus input/output line 13
HD14	66	I/O	host interface data bus input/output line 14
HD15	67	I/O	host interface data bus input/output line 15
DGND6	68	–	digital ground 6
$\overline{DA0}$/CMD	69	I	host interface data input (active LOW)/command select input host interface address line 0
DA1	70	I	ATAPI address line input 1
DA2/EJECT	71	I	ATAPI address line input 2
CS2/SELRQ	72	I	ATAPI chip select input 2
IOCS16	73	O	ATAPI 16-bit data select output
V_{DDD2}	74	–	digital supply voltage 2 (5 V)
RA0	75	O	buffer RAM address bus output line 0
RA1	76	O	buffer RAM address bus output line 1
RA2	77	O	buffer RAM address bus output line 2

SYMBOL	PIN	I/O	DESCRIPTION
RA3	78	O	buffer RAM address bus output line 3
RA4	79	O	buffer RAM address bus output line 4
RA5	80	O	buffer RAM address bus output line 5

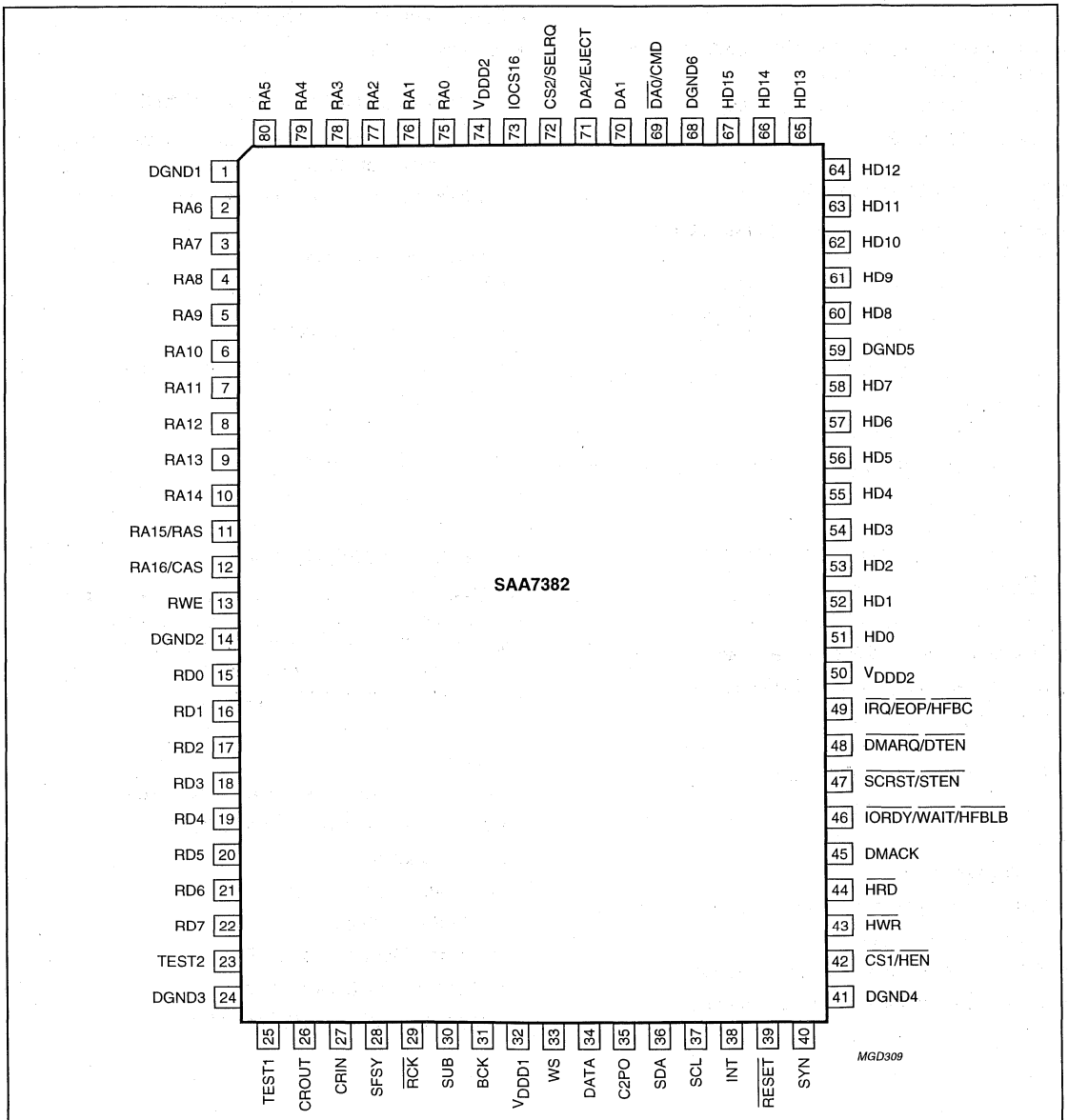


Fig.2 Pin configuration.

1 FEATURES

1.1 General

- Single chip digital solution for an 8 × speed CD-ROM controller chip
- 10 Mbytes/s NCR53CF94 equivalent SCSI controller included
- High-speed 80C32 microcontroller with 256 × 8 scratch-pad SRAM included
- High performance CD-ROM interface logic
- 128 pin QFP package.

1.2 53CF94 SCSI controller

- Separate clock input to allow operation up to the maximum 10 Mbytes/s
- Fast synchronous SCSI-2 compatible
- 24-bit transfer counter for single transfers up to 16 Mbytes
- High-speed 16-bit DMA interface to the buffer manager DRAM
- On-chip 48 mA SCSI drivers
- Software compatible with members of the 53C90 family
- Allows for SCAM support.

1.3 80C32 high-speed microcontroller

- 33.87 MHz full system speed operation
- Three timers/event counters
- Programmable full duplex serial channel
- Eight general purpose microcontroller I/O pins
- External program ROM.

1.4 Front-end interface logic

- Full 8 × speed hardware operation
- Block decoder
- Sector sequencer
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- 212 ms watch-dog timer
- Sub-code interface with synchronization
- C-flag interface for absolute time stamp.

1.5 Buffer controller

- Ten level arbitration logic
- Utilizes low cost 70 ns DRAMs
- Page mode DRAM access for high-speed error correction and SCSI data transfer
- Data organization by 3 kbyte frames
- 256 kbyte or 1 Mbyte DRAM supported.

1.6 Hardware third-level error correction

- Third-level correction provides superior performance in unfavourable conditions
- Full hardware error correction to reduce microcontroller overhead
- Corrections are automatically written to the DRAM frame buffer.

1.7 Additional product support

- All control registers mapped into 80C32 special function memory space
- Dedicated S2B interface UART
- Input clock synthesizer
- Red book audio pass through.

2 GENERAL DESCRIPTION

The SAA7385 is a high integration ASIC that incorporates all of the digital electronics necessary to connect a CD decoder to a SCSI host. An 80C32 microcontroller and a 53CF94 SCSI controller are embedded in the ASIC. The following functions are supported:

- Input clock doubler
- Block decoder
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- Red book audio pass through to SCSI
- Buffer manager
- Third-level error correction
- Sub-code and Q-channel support
- Dedicated S2B interface UART
- Embedded 80C32 microcontroller
- Embedded 53CF94 SCSI controller.

The SAA7385 uses a 33.8688 MHz clock and is capable of accepting data at eight times (n = 8 or 1.4 Mbytes/s) the normal CD-ROM data rate.

Third level error correction hardware is included to improve the correction efficiency of the system. The buffer manager hardware utilizes a ten-level arbitration unit and can stop the clock to the microcontroller to emulate a wait condition when necessary.

The SAA7385 comprises five major functional blocks:

- The 80C32 microcontroller is an industry standard core
- The 53CF94 is an industry standard core
- The front-end block connects to the external CD-60 based decoder and fully processes the incoming data stream to provide bytes of data that are stored in the external buffer
- The buffer manager block provides the address generation and timing control for the external DRAM buffer
- The ECC block performs the error correction functions in hardware on the data in the DRAM buffer.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	–55	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7385GP	SQFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 14 × 20 × 2.8 mm	SOT387-2

5 BLOCK DIAGRAM

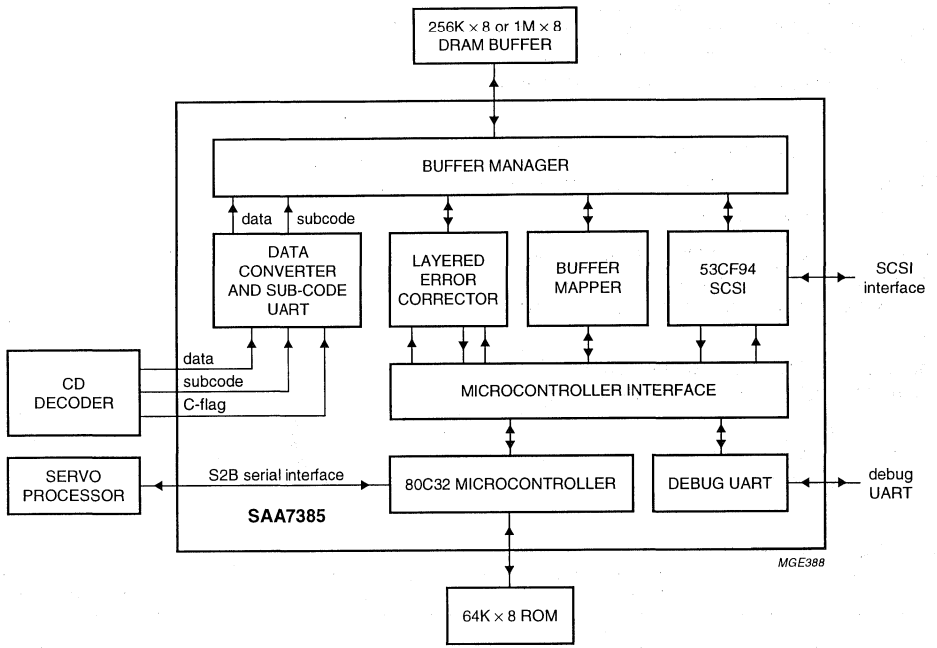


Fig.1 Block diagram (simplified).

6 PINNING

All input, output and bidirectional signals are TTL level unless otherwise stated (Pull-Down = PD25 = 25 µA; Pull-Up = PU25 = 25 µA, PU400 = 400 µA; Slew = S2 = 2 mA, S4 = 4 mA; CMOS slew = CMOS S2 = CMOS 2 = 2 mA; SCSI pad = SCSI = 48 mA).

SYMBOL	PIN	I/O	PAD	DESCRIPTION
DA2	1	O	S4	DRAM address bus; bit DA2
DA3	2	O	S4	DRAM address bus; bit DA3
DA4	3	O	S4	DRAM address bus; bit DA4
V_{SS1}	4	–	–	ground 1
DA5	5	O	S4	DRAM address bus; bit DA5
DA6	6	O	S4	DRAM address bus; bit DA6
DA7	7	O	S4	DRAM address bus; bit DA7
DA8	8	O	S4	DRAM address bus; bit DA8
DA9	9	O	S4	DRAM address bus; bit DA9
V_{DD1}	10	–	–	power supply 1

SYMBOL	PIN	I/O	PAD	DESCRIPTION
$\overline{RAS}$	11	O	S4	DRAM row address section; active LOW
$\overline{CAS}$	12	O	S4	DRAM column address selection; active LOW
$\overline{DWR}$	13	O	S4	DRAM write; active LOW
$\overline{DOE}$	14	O	S4	DRAM output enable; active LOW
V_{SS2}	15	–	–	ground 2
DD0	16	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD0
DD1	17	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD1
DD2	18	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD2
DD3	19	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD3
V_{DD2}	20	–	–	power supply 2
DD4	21	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD4
DD5	22	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD5
DD6	23	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD6
DD7	24	I/O	4 mA, Schmitt, PD25	DRAM data bus; bit DD7
V_{SS3}	25	–	–	ground 3
$\overline{LED}$	26	O	24 mA, CMOS test	panel LED; active LOW; WTGCTL(4)
$\overline{TRAYSW}$	27	I	Schmitt, PU25	active LOW when tray is in
$\overline{EJECT}$	28	I	Schmitt, PU25	opens tray; active LOW
LQDATA	29	O	2 mA	serial data to DAC
LWCLK	30	O	2 mA	word strobe to DAC
V_{SS4}	31	–	–	ground 4
SCLK	32	O	2 mA	data serial clock
V_{SS5}	33	–	–	ground 5
SYSRES	34	O	2 mA, PU25	system reset; OR of $\overline{POR}$, $\overline{SCSIRST}$ and watch-dog timer
CFLAG	35	I	Schmitt, PU400	C1 and C2 status
$\overline{CPR}$	36	O	2 mA	S2B interface ready to accept data; active LOW
$\overline{SPR}$	37	I	Schmitt	S2B interface ready to send data; active LOW
$\overline{SKIPFWD}$	38	I	Schmitt, PU25	skip forwards; active LOW; RDSW(3)
$\overline{SKIPBACK}$	39	I	Schmitt, PU25	skip backwards; active LOW; RDSW(2)
SCSICLK	40	I	standard	SCSI interface clock
V_{DD3}	41	–	–	power supply 3
AD0	42	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD0
AD1	43	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD1
AD2	44	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD2
AD3	45	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD3
AD4	46	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD4
AD5	47	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD5
AD6	48	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD6
AD7	49	I/O	S4, Schmitt	microcontroller multiplexed data bus; bit AD7
V_{SS6}	50	–	–	ground 6
LA0	51	O	CMOS S2, PU25	EPROM latched lower address; bit LA0

SYMBOL	PIN	I/O	PAD	DESCRIPTION
LA1	52	O	CMOS S2, PU25	EPROM latched lower address; bit LA1
LA2	53	O	CMOS S2, PU25	EPROM latched lower address; bit LA2
LA3	54	O	CMOS S2, PU25	EPROM latched lower address; bit LA3
V_{DD4}	55	–	–	power supply 4
LA4	56	O	CMOS S2, PU25	EPROM latched lower address; bit LA4
LA5	57	O	CMOS S2, PU25	EPROM latched lower address; bit LA5
LA6	58	O	CMOS S2, PU25	EPROM latched lower address; bit LA6
LA7	59	O	CMOS S2, PU25	EPROM latched lower address; bit LA7
V_{SS7}	60	–	–	ground 7
A8	61	O	CMOS S2, PU25	EPROM upper address; bit A8
A9	62	O	CMOS S2, PU25	EPROM upper address; bit A9
A10	63	O	CMOS S2, PU25	EPROM upper address; bit A10
A11	64	O	CMOS S2, PU25	EPROM upper address; bit A11
A12	65	O	CMOS S2, PU25	EPROM upper address; bit A12
A13	66	O	CMOS S2, PU25	EPROM upper address; bit A13
A14	67	O	CMOS S2, PU25	EPROM upper address; bit A14
A15	68	O	CMOS S2, PU25	EPROM upper address; bit A15
$\overline{PSEN}$	69	O	CMOS 2, PU25	program store enable; active LOW
V_{SS8}	70	–	–	ground 8
$\overline{IO}$	71	I/O	SCSI	SCSI phase signal, active LOW
$\overline{REQ}$	72	I/O	SCSI	SCSI request, active LOW
$\overline{CD}$	73	I/O	SCSI	SCSI phase signal, active LOW
$\overline{SEL}$	74	I/O	SCSI	SCSI select, active LOW
V_{SS9}	75	–	–	ground 9
$\overline{MSG}$	76	I/O	SCSI	SCSI phase signal, active LOW
$\overline{ACK}$	77	I/O	SCSI	SCSI acknowledge, active LOW
$\overline{BSY}$	78	I/O	SCSI	SCSI busy, active LOW
V_{SS10}	79	–	–	ground 10
$\overline{ATN}$	80	I/O	SCSI	output in initiator mode; input in target mode, active LOW
V_{DD5}	81	–	–	power supply 5
$\overline{SDP}$	82	I/O	SCSI	SCSI parity, active LOW
SD7	83	I/O	SCSI	SCSI data bus; bit SD7
SD6	84	I/O	SCSI	SCSI data bus; bit SD6
SD5	85	I/O	SCSI	SCSI data bus; bit SD5
V_{SS11}	86	–	–	ground 11
SD4	87	I/O	SCSI	SCSI data bus; bit SD4
SD3	88	I/O	SCSI	SCSI data bus; bit SD3
SD2	89	I/O	SCSI	SCSI data bus; bit SD2
SD1	90	I/O	SCSI	SCSI data bus; bit SD1
SD0	91	I/O	SCSI	SCSI data bus; bit SD0
V_{SS12}	92	–	–	ground 12

SYMBOL	PIN	I/O	PAD	DESCRIPTION
RXS2B	93	I	Schmitt, PU25	S2B interface receive
TXS2B	94	O	4 mA	S2B interface transmit
$\overline{\text{TRAYIN}}$	95	I/O	4 mA, PD25	tray extend control; active LOW (general purpose signal)
$\overline{\text{TRAYOUT}}$	96	I/O	4 mA, PD25	tray retract control; active LOW (general purpose signal)
$\overline{\text{SCSIRST}}$	97	I	Schmitt	SCSI reset, active LOW; also causes a system reset
$\overline{\text{POR}}$	98	I	CMOS	power-on reset; active LOW
V_{DD6}	99	–	–	power supply 6
UC_PORT1.7	100	I/O	CMOS 2, PU25	drive speed select; microcontroller port 1.7
RAB_MUSB	101	I/O	CMOS 2, PU25	RD/WR, acknowledge; microcontroller port 1.2
NRST_SEQ	102	I/O	CMOS 2, PU25	reset to engine; microcontroller port 1.5
UC_PORT1.4	103	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.4
UC_PORT1.3	104	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.3
UC_PORT1.1	105	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.1
$\overline{\text{HOMESW}}$	106	I/O	2 mA, PU25	actuator sled home; active LOW; microcontroller port 1.0
$\overline{\text{PLAY}}$	107	I	Schmitt	laser on and focused status; active LOW; RDSW(4)
UC_PORT1.6	108	I/O	CMOS 2, PU25	general purpose microcontroller I/O port; port 1.6
V_{SS13}	109	–	–	ground 13
GPI1	110	I	Schmitt, PU25	general purpose input; microcontroller port 3.4
GPI2	111	I	Schmitt, PU25	general purpose input; microcontroller port 3.5
$\overline{\text{KILL}}$	112	I	Schmitt, PU25	shut off audio; active LOW
TXICE	113	O	4 mA	debug UART output; from 80C32 serial port
RXICE	114	I	Schmitt, PU25	debug UART input; to 80C32 serial port
RXSUB	115	I	Schmitt, PU25	sub-code input
V_{DD7}	116	–	–	power supply 7
OSCIN	117	I	standard	master input clock; 34 or 16 MHz
V_{SS14}	118	–	–	ground 14
CLAB	119	I	Schmitt	clock
V_{SS15}	120	–	–	ground 15
DAAB	121	I	Schmitt	data
WSAB	122	I	Schmitt	word strobe
EFAB	123	I	Schmitt	error flag
CLK34	124	O	2 mA	34 MHz output clock
TEST	125	I	Schmitt, PD25	test pin; must be ground
V_{SS16}	126	–	–	ground 16
DA0	127	O	S4	DRAM address bus; bit DA0
DA1	128	O	S4	DRAM address bus; bit DA1

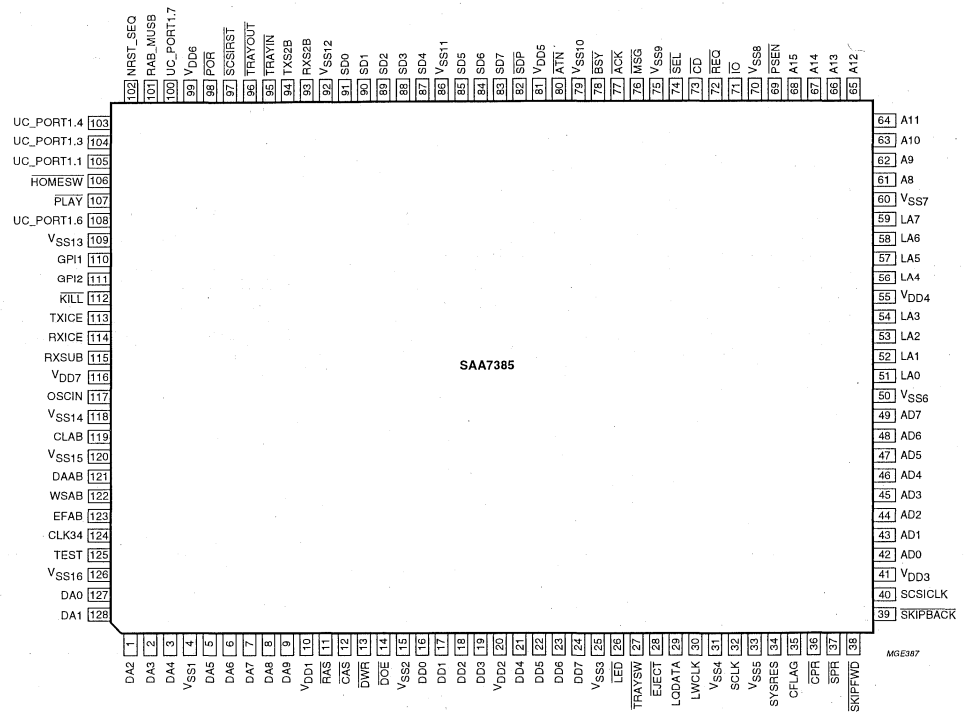


Fig.2 Pin configuration.

Error correction and host interface IC for CD-ROM (ELM)

SAA7388

1 FEATURES

- CD-ROM (Mode 1) and CD-I (Mode 2 - Form 1 and Form 2) formats supported
- Real-time error detection and correction in hardware
- Suitable for octal speed, n = 8.
- Maximum host transfer burst rate of 13.3 Mbyte/s
- Corrects two errors per symbol with erasure correction
- 36 kbit of on-chip error correction buffer RAM
- 12-byte command FIFO and 12-byte status FIFO
- Compatible with the Advanced Technology Attachment (ATA) register set and the Advanced Technology Attachment Program Interface (ATAPI) command set
- Operates with popular memories. (up to 128 kbyte SRAM; 1 to 16 Mbit DRAM, different speed grades, nibble or byte wide)
- Interface to Integrated Drive Electronics (IDE) bus without external bus drivers
- Q-to-W subcode buffering, de-interleaving and correction are supported
- Device can operate with audio RAMs. A RAM test allows bad segments to be identified.

2 GENERAL DESCRIPTION

The SAA7388 decoder is a block decoder buffer manager for high-speed CD-ROM applications that integrates real-time error correction and detection and host interface data transfer functions into a single chip.

The SAA7388 has an on-chip 36-kbit memory. This memory is used as a buffer memory for error and erasure corrections. The chip also has a buffer memory interface thus enabling the connection of SRAM up to 128 kbytes, or DRAM up to 16 Mbits. The on-chip memory is sufficient to buffer 1 sector of data. The external memory can buffer many more, depending on memory size.

The error corrector of the SAA7388 can perform 2-pass error correction in real-time. Buffer memory for this correction is integrated on-chip.

The SAA7388 has an host interface that is compatible with the SANYO LC89510 or OAK OTI-012 and also compatible with the ATA/IDE/ATAPI hard disc interface bus. (All ATAPI registers are present in hardware).

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDD1}	digital supply voltage 1	3.0	3.3	3.6	V
V_{DDD2}	digital supply voltage 2	4.5	5	5.5	V
I_{DDD}	supply current	–	60	–	mA
f_{clk}	clock frequency	15.2	48	50.4	MHz
T_{amb}	operating ambient temperature	0	–	+70	°C
T_{stg}	storage temperature	−55	–	+125	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7388GP	QFP80	plastic quad flat package; 80 leads; lead length 1.95 mm; body 14 × 20 × 2.8 mm	SOT318-2

5 BLOCK DIAGRAM

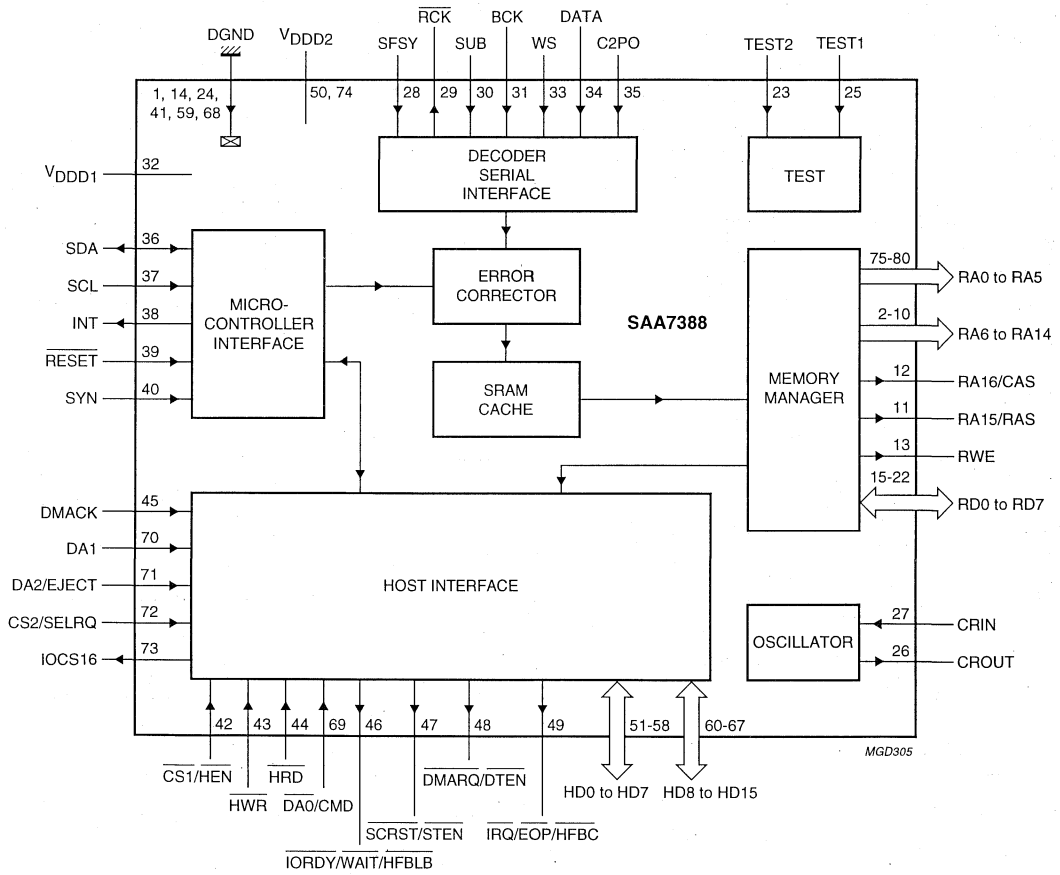


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
DGND1	1	–	digital ground 1
RA6	2	O	buffer RAM address bus output line 6
RA7	3	O	buffer RAM address bus output line 7
RA8	4	O	buffer RAM address bus output line 8
RA9	5	O	buffer RAM address bus output line 9
RA10	6	O	buffer RAM address bus output line 10
RA11	7	O	buffer RAM address bus output line 11 (SRAM) only
RA12	8	O	buffer RAM address bus output line 12 (SRAM) only
RA13	9	O	buffer RAM address bus output line 13 (SRAM) only
RA14	10	O	buffer RAM address bus output line 14 (SRAM) only
RA15/RAS	11	O	buffer RAM address bus output line 15 (SRAM) or RAS (DRAM)
RA16/CAS	12	O	buffer RAM address bus output line 16 (SRAM) or CAS (DRAM)
RWE	13	O	buffer RAM write enable output
DGND2	14	–	digital ground 2
RD0	15	I/O	buffer RAM data bus bidirectional line 0
RD1	16	I/O	buffer RAM data bus bidirectional line 1
RD2	17	I/O	buffer RAM data bus bidirectional line 2
RD3	18	I/O	buffer RAM data bus bidirectional line 3
RD4	19	I/O	buffer RAM data bus bidirectional line 4
RD5	20	I/O	buffer RAM data bus bidirectional line 5
RD6	21	I/O	buffer RAM data bus bidirectional line 6
RD7	22	I/O	buffer RAM data bus bidirectional line 7
TEST2	23	I	test input 2
DGND3	24	–	digital ground 3
TEST1	25	I	test input 1
CROUT	26	O	clock oscillator output
CRIN	27	I	clock oscillator input
SFSY	28	I	serial subcode input frame sync input
$\overline{\text{RCK}}$	29	O	serial subcode clock output (active LOW)
SUB	30	I	serial input for Q-to-W subcode input
BCK	31	I	serial interface bit clock input
V_{DDD1}	32	–	digital supply voltage 1 (3.3 V)
WS	33	I	serial interface word clock input
DATA	34	I	serial data input
C2PO	35	I	serial interface flag input
SDA	36	I/O	sub-CPU serial data input/output
SCL	37	I	sub-CPU serial clock input
INT	38	O	sub-CPU open-collector interrupt output
$\overline{\text{RESET}}$	39	I	power-on reset input (active LOW)
SYN	40	I	sync signal input from sub-CPU

SYMBOL	PIN	I/O	DESCRIPTION
DGND4	41	–	digital ground 4
$\overline{CS1}/\overline{HEN}$	42	I	host interface enable input (active LOW)
$\overline{HWR}$	43	I	host interface write enable input (active LOW)
$\overline{HRD}$	44	I	host interface read enable input (active LOW)
DMACK	45	I	DMA acknowledge input
$\overline{IORDY}/\overline{WAIT}/\overline{HFBLB}$	46	O	host interface wait output (active LOW); 3-state control
$\overline{SCRST}/\overline{STEN}$	47	O	host interface status enable output ATAPI sub-CPU reset signal (active LOW)
$\overline{DMARQ}/\overline{DTEN}$	48	O	ATAPI DMA request host interface data enable output (active LOW); 3-state control
$\overline{IRQ}/\overline{EOP}/\overline{HFBC}$	49	O	host interface end of process flag output ATAPI host interrupt request (active LOW); 3-state control
V_{DDD2}	50	–	digital supply voltage 2 (5 V)
HD0	51	I/O	host interface data bus input/output line 0
HD1	52	I/O	host interface database input/output line 1
HD2	53	I/O	host interface database input/output line 2
HD3	54	I/O	host interface data bus input/output line 3
HD4	55	I/O	host interface data bus input/output line 4
HD5	56	I/O	host interface data bus input/output line 5
HD6	57	I/O	host interface data bus input/output line 6
HD7	58	I/O	host interface data bus input/output line 7
DGND5	59	–	digital ground 5
HD8	60	I/O	host interface data bus input/output line 8
HD9	61	I/O	host interface data bus input/output line 9
HD10	62	I/O	host interface data bus input/output line 10
HD11	63	I/O	host interface data bus input/output line 11
HD12	64	I/O	host interface data bus input/output line 12
HD13	65	I/O	host interface data bus input/output line 13
HD14	66	I/O	host interface data bus input/output line 14
HD15	67	I/O	host interface data bus input/output line 15
DGND6	68	–	digital ground 6
$\overline{DA0}/CMD$	69	I	host interface data input (active LOW)/command select input host interface address line 0
DA1	70	I	ATAPI address line input 1
DA2/EJECT	71	I	ATAPI address line input 2
CS2/SELRQ	72	I	ATAPI chip select input 2
IOCS16	73	O	ATAPI 16-bit data select output
V_{DDD2}	74	–	digital supply voltage 2 (5 V)
RA0	75	O	buffer RAM address bus output line 0
RA1	76	O	buffer RAM address bus output line 1
RA2	77	O	buffer RAM address bus output line 2

SYMBOL	PIN	I/O	DESCRIPTION
RA3	78	O	buffer RAM address bus output line 3
RA4	79	O	buffer RAM address bus output line 4
RA5	80	O	buffer RAM address bus output line 5

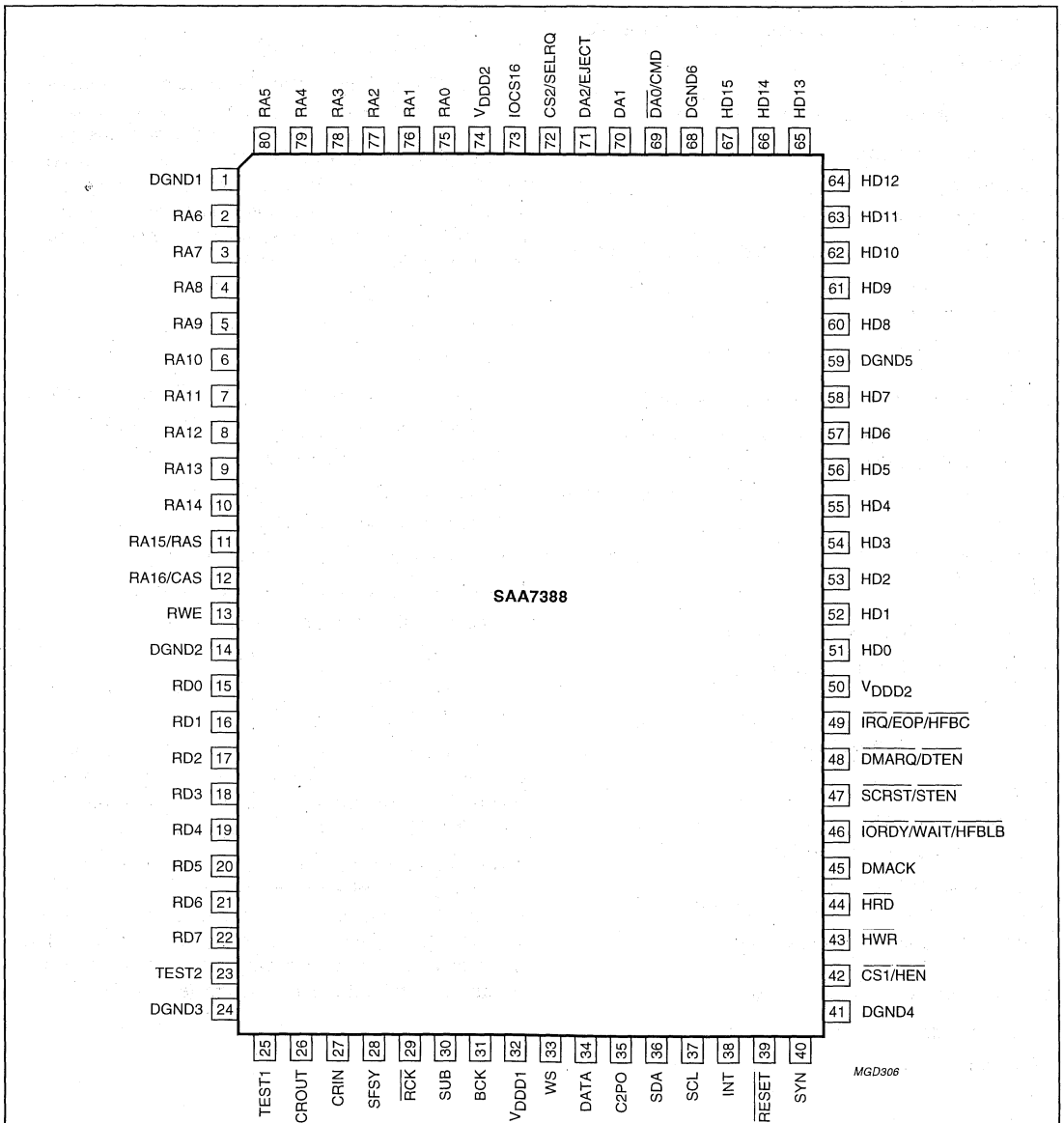


Fig.2 Pin configuration.

High performance Compact Disc-Recordable (CD-R) controller

SAA7390

1 FEATURES

1.1 General

- 8× speed CD-ROM, 4× speed Compact Disc-Recordable (CD-R) controller
- 16.9 Mbytes/s burst rate to host controller
- High performance CD-ROM and CD-R interface logic
- 128 pin QFP package.

1.2 Interface logic (CD-ROM operation)

- Full 8× speed hardware operation
- Block decoder
- Sector sequencer
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- 212 ms watch-dog timer
- Sub-code interface with synchronization
- C-flag interface for absolute time stamp.

1.3 Hardware third-level error correction

- Third-level correction provides superior performance in unfavourable conditions
- Full hardware error correction to reduce microcontroller overhead
- Corrections are automatically written to the DRAM frame buffer.

1.4 Interface logic (CD-R operation)

- Block encoder (using a modified CDB2).

1.5 DRAM buffer controller (256 kbytes × 8, 1 Mbyte × 8, 4 Mbytes × 8)

- DRAM buffer manager
- Ten level arbitration logic
- Utilizes low cost 70 ns DRAMs
- Page mode DRAM access for high-speed error correction and host interface data transfers
- Data organization by 3 kbytes frames.

1.6 Additional product support

- Input clock doubler
- All control registers mapped into 80C32 special function memory space
- Red book audio pass through to host interface
- Sub-code and Q-channel support
- Dedicated Serial Peripheral Interface (SPI)
- Third level error correction and encoding
- 80C32 microcontroller interface
- 53CF90 or 53CF92A/B fast SCSI processor interface (may also use ATAPI processor).

2 GENERAL DESCRIPTION

The SAA7390 is a high integration ASIC that incorporates all of the logic necessary to connect a CD-60 based decoder to a SCSI or ATAPI host. It also supports a data path from the host to the CDCEP (compact disc encoder) for CD-R applications. An 80C32 microcontroller and a 53CF94/92A (or an ATAPI interface device) are required to provide the full block encode/decode functions. The following functions are supported:

- Input clock doubler
- Block encoder (using a modified CDB2)
- Block decoder
- CRC checking of Mode 1 and Mode 2, Form 1 sectors
- Red book audio pass through to SCSI or ATAPI
- Sub-code and Q-channel support
- Dedicated S2B interface UART
- Dedicated SPI interface UART
- Up to 4 Mbytes DRAM buffer manager
- Third-level error correction and encoding
- Automatic storage of audio and data
- 80C32 microcontroller interface
- 53CF90 or 53CF92A/B fast SCSI or Wapiti ATAPI processor interface.

The SAA7390 uses a 33.8688 MHz clock and is capable of accepting data at eight times (n = 8 or 1.4 Mbytes/s) the normal CD-ROM data rate. The minimum host burst rate capability of the SAA7390 is 5 Mbytes/s.

Third level error correction hardware is included to improve the correction efficiency of the system. The buffer manager hardware utilizes a ten-level arbitration unit and can stop the clock to the static microcontroller to emulate a wait condition when necessary. The host interface is capable of burst rates to 16.9 Mbytes/s.

The SAA7390 comprises four major functional blocks:

- The front-end block connects to the external CD-60 based decoder and fully processes the incoming data stream
- The buffer manager block provides the address generation and timing control for the external DRAMs
- The ECC block performs the error correction functions in hardware on the data stored in the DRAM buffer.
- The block encoder function (realized via a modified CDB2) serializes the data from the buffer, appends the sync pattern, header, sub-header, third level ECC parity and EDC bytes as necessary, performs the required scrambling and outputs them to the CDCEP using a special data clock (98 clock cycles per word selection period).

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	4.5	5.0	5.5	V
T_{amb}	operating ambient temperature	0	–	70	°C
T_{stg}	storage temperature	–55	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7390GP[1]	SQFP128	plastic quad flat package; 128 leads (lead length 1.6 mm); body 14 × 20 × 2.8 mm	SOT387-2

Note

1. This device uses a Symbios logic package.

5 BLOCK DIAGRAM

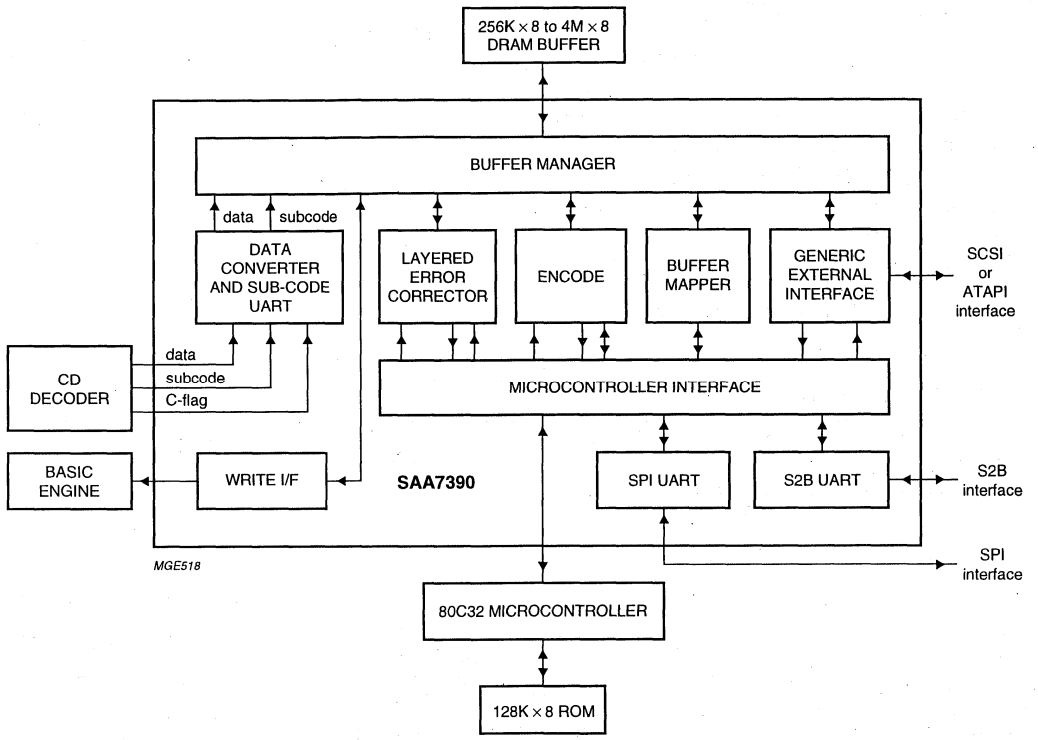


Fig.1 Block diagram (simplified).

6 PINNING

All input and bidirectional signals are TTL level with Schmitt-trigger logic, with the exception of OSCIN. All output signals are TTL levels unless otherwise stated. (PD = internal pull-down; PU = internal pull-up).

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DA0	1	O		DRAM address bus; bit DA0
DA1	2	O		DRAM address bus; bit DA1
DA2	3	O		DRAM address bus; bit DA2
V_{SS1}	4	–		ground 1
DA3	5	O		DRAM address bus; bit DA3
DA4	6	O		DRAM address bus; bit DA4
DA5	7	O		DRAM address bus; bit DA5
V_{SS2}	8	–		ground 2
DA6	9	O		DRAM address bus; bit DA6

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
DA7	10	O		DRAM address bus; bit DA7
V_{DD1}	11	–		power supply 1
DA8	12	O		DRAM address bus; bit DA8
DA9	13	O		DRAM address bus; bit DA9
DA10	14	O		DRAM address bus; bit DA10
$\overline{RAS}$	15	O		DRAM row address section; active LOW
$\overline{CAS}$	16	O		DRAM column address selection; active LOW
$\overline{DWR}$	17	O		DRAM write; active LOW
$\overline{DOE}$	18	O		DRAM output enable; active LOW
DD0	19	I/O	PD	DRAM data bus; bit DD0
V_{DD2}	20	–		power supply 2
DD1	21	I/O	PD	DRAM data bus; bit DD1
DD2	22	I/O	PD	DRAM data bus; bit DD2
DD3	23	I/O	PD	DRAM data bus; bit DD3
DD4	24	I/O	PD	DRAM data bus; bit DD4
V_{SS3}	25	–		ground 3
DD5	26	I/O	PD	DRAM data bus; bit DD5
DD6	27	I/O	PD	DRAM data bus; bit DD6
DD7	28	I/O	PD	DRAM data bus; bit DD7
COM_IN	29	I		serial data in from basic engine
COM_OUT	30	O		serial data out to basic engine
COM_CLK	31	O		serial data clock
COM_ACK	32	I		serial data acknowledge
$\overline{TRAYSW}$	33	I	PU	active LOW when tray is in
$\overline{EJECT}$	34	I	PU	opens tray; active LOW
LQDATA	35	O		latched qualified data
LWCLK	36	O		latched word clock
V_{DD3}	37	–		power supply 3
$\overline{LED}$	38	O	CMOS; 24 mA	panel LED; active LOW; open drain; 24 mA (min.) sink capability
V_{SS4}	39	–		ground 4
SCLK	40	O		audio data clock
V_{SS5}	41	–		ground 5
SYSRES	42	O		system reset; active HIGH
$\overline{SYSRES}$	43	O		system reset; active LOW
V_{DD4}	44	–		power supply 4
GPIO3	45	I/O	PD	general purpose input/output 3
GPIO4	46	I/O	PD	general purpose input/output 4
$\overline{VOLUP}$	47	I	PU	volume up; active LOW
$\overline{VOLDN}$	48	I	PU	volume down; active LOW
UC_AD0	49	I/O		microprocessor multiplexed address/data bus; bit UC_AD0
UC_AD1	50	I/O		microprocessor multiplexed address/data bus; bit UC_AD1

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
UC_AD2	51	I/O		microprocessor multiplexed address/data bus; bit UC_AD2
UC_AD3	52	I/O		microprocessor multiplexed address/data bus; bit UC_AD3
V_{SS6}	53	–		ground 6
UC_AD4	54	I/O		microprocessor multiplexed address/data bus; bit UC_AD4
UC_AD5	55	I/O		microprocessor multiplexed address/data bus; bit UC_AD5
UC_AD6	56	I/O		microprocessor multiplexed address/data bus; bit UC_AD6
UC_AD7	57	I/O		microprocessor multiplexed address/data bus; bit UC_AD7
V_{DD5}	58	–		power supply 5
UC_LA0	59	O		latched lower address; bit UC_LA0
UC_LA1	60	O		latched lower address; bit UC_LA1
UC_LA2	61	O		latched lower address; bit UC_LA2
V_{SS7}	62	–		ground 7
UC_LA3	63	O		latched lower address; bit UC_LA3
UC_LA4	64	O		latched lower address; bit UC_LA4
UC_LA5	65	O		latched lower address; bit UC_LA5
UC_LA6	66	O		latched lower address; bit UC_LA6
UC_LA7	67	O		latched lower address; bit UC_LA7
V_{SS8}	68	–		ground 8
PCLK	69	O		33.8688 MHz microprocessor clock
V_{DD6}	70	–		power supply 6
ALE	71	I		address latch enable
$\overline{UC\_WR}$	72	I		write enable
$\overline{UC\_RD}$	73	I		read enable
$\overline{INT}$	74	O	CMOS	interrupt to microcontroller; active LOW; open drain
UC_A8	75	I		upper address; bit UC_A8
UC_A9	76	I		upper address; bit UC_A9
UC_A10	77	I		upper address; bit UC_A10
SYS_SYNC	78	I		system synchronization from basic engine
UC_A11	79	I		upper address; bit UC_A11
UC_A12	80	I		upper address; bit UC_A12
UC_A13	81	I		upper address; bit UC_A13
COM_SYNC	82	I		communication synchronization from basic engine
UC_A14	83	I		upper address; bit UC_A14
UC_A15	84	I		upper address; bit UC_A15
SD0	85	I/O		internal data bus; bit SD0
V_{DD6}	86	–		power supply 6
SD1	87	I/O		internal data bus; bit SD1
SD2	88	I/O		internal data bus; bit SD2
V_{SS9}	89	–		ground 9
SD3	90	I/O		internal data bus; bit SD3
SD4	91	I/O		internal data bus; bit SD4

SYMBOL	PIN	I/O	TYPE	DESCRIPTION
SD5	92	I/O		internal data bus; bit SD5
SD6	93	I/O		internal data bus; bit SD6
SD7	94	I/O		internal data bus; bit SD7
V_{SS10}	95	–		ground 10
DREQ	96	I	PD	DMA request
$\overline{DACK}$	97	O		DMA acknowledge; active LOW
$\overline{HOSTRD}$	98	O		read enable; active LOW
$\overline{HOSTWR}$	99	O		write enable; active LOW
$\overline{HOSTSEL}$	100	O		chip select; active LOW
CSAB	101	I		word strobe for write data
CCLAB	102	I		clock for write data
CDAAB	103	O		write data stream
RXS2B	104	I	PU	receive data
TXS2B	105	O		transmit data
$\overline{CPR}$	106	O		ready to accept data; active LOW
$\overline{SCSIRST}$	107	I		reset from SCSI bus; active LOW
$\overline{POR}$	108	I		power-on reset; active LOW
TCL_GPIO1	109	I/O	PD	general purpose input/output 1 (also used as test-mode clock)
$\overline{SPR}$	110	I		ready to send data; active LOW
TDA_GPIO2	111	I/O	PD	general purpose input/output 2 (also used as test-mode data)
$\overline{HFD}$	112	I		laser on and focused status; active LOW
$\overline{KILL}$	113	I	PU	mute audio; active LOW
V_{SS11}	114	–		ground 11
MCOUT	115	O		motor control output from PWM
MCIN	116	I	PD	motor control input from decoder
RXSUB	117	I	PU	sub-code input
CFLAG	118	I	PU	C1 and C2 status
V_{SS12}	119	–		ground 12
OSCIN	120	I		input clock from decoder
V_{DD7}	121	–		power supply 7
CLAB	122	I		clock input
DAAB	123	I		data input
WSAB	124	I		word strobe input
EFAB	125	I		error flags
V_{SS13}	126	–		ground 13
CLK34	127	O		33.8688 MHz output clock
V_{DD8}	128	–		power supply 8

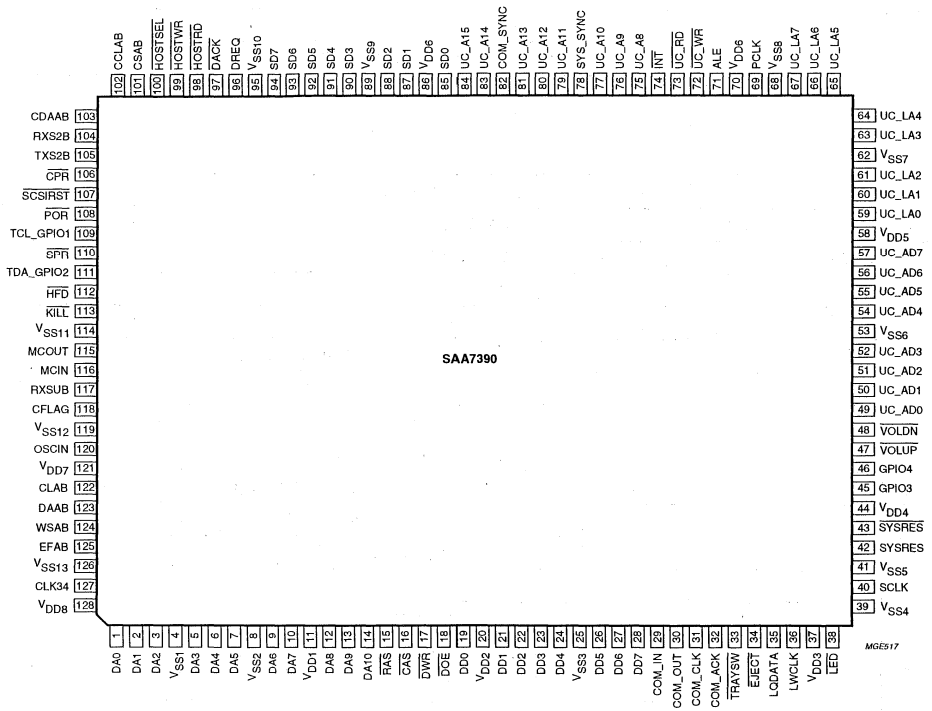


Fig.2 Pin configuration.

Car radio Digital Signal Processor (CDSP) SAA7707H

1 FEATURES

1.1 Hardware

- Bitstream 3rd-order Sigma-Delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filters
- Digital-to-Analog Converters (DACs)with four times oversampling and noise shaping
- Digital stereo decoder
- Improved digital Interference Absorption Circuit (IAC)
- RDS processing with optional 16-bit buffer via separate channel (two-tuner radio possible)
- Auxiliary analog CD input (CD-walkman, speech, economic CD-changer, etc.)
- Two separate full I²S-bus CD and DCC high performance interfaces
- Expandable with additional Digital Signal Processors (DSPs) for sophisticated features through an I²S-bus gateway
- Audio output short-circuit protected
- I²C-bus controlled
- Analog tape input
- Operating ambient temperature from –40 to +85 °C.

1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation and Dolby level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Dynamic loudness or bass boost
- Stereo one-band parametric equalizer
- Audio level meter for an automatic leveller (in combination with microcontroller)
- Tape equalization (DCC analog playback)
- Music Search detection for Tape (MSS)
- Pause detection for RDS updates
- Dolby-B tape noise reduction
- Adjustable dynamics compressor
- CD and DCC de-emphasis processing
- Signal level, noise and multi-path detection for RDS (I²C-bus command)
- Improved AM reception.

2 APPLICATIONS

- Car radio
- Car audio systems.

3 GENERAL DESCRIPTION

The SAA7707H performs all the signal functions in front of the power amplifiers and behind the AM and FMMPX demodulation of a car radio or the tape input.
These functions are:

- Interference absorption
- Stereo decoding
- RDS decoding
- FM and AM weak signal processing (soft mute, sliding stereo, etc.)
- Dolby-B tape noise reduction
- The audio controls (volume, balance, fader, tone and dynamics compression).

Some functions have been implemented in hardware (stereo decoder, RDS decoder and IAC) and are not freely programmable. Digital audio signals from external sources with I²S-bus formats are accepted. There are four independent analog output channels. This enables, in special system configurations, separate tone and equalization control for front and rear speakers.

The CDSP contains a basic program that enables a set with:

- AM/FM reception
- Sophisticated FM weak signal functions
- Music Search detection for Tape (MSS)
- Dolby-B tape noise reduction system
- CD play with compressor function
- Separate bass and treble tone control and fader/balance control.

For high-end sets with special and more sophisticated features, an additional Digital Signal Processor (DSP) can be connected. Examples of such features are:

- Noise-dependent volume control
- 10-band graphic equalizer
- Audio spectrum analyzer on display
- Signal delay for concert hall effects.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(tot)}$	total DC supply voltage	all supply pins	4.75	5	5.5	V
$I_{DDD(tot)}$	total DC supply current	maximum activity of the DSP; f_{xtal} = 36 MHz	–	160	200	mA
P_{tot}	total power dissipation	maximum activity of the DSP; f_{xtal} = 36 MHz	–	0.8	1.1	W
S/N	level ADC signal-to-noise ratio	RMS value; unweighted; B = 0 to 29 kHz; maximum input	48	54	–	dB
	ADC signal-to-noise ratio	not multiplexed; B = 19 kHz; V_i = 1 V (RMS)	81	85	–	dB
		multiplexed; unweighted; B = 19 kHz; 1 V (RMS)	72	76	–	dB
	ADC signal-to-noise ratio for FM-RDS	RMS value; B = 6 kHz; unweighted; f_c = 57 kHz	56	–	–	dB
V_{iFS}	ADC full scale input voltage	V_{DDA1} = 4.75 to 5.5 V	$1.05V_{DDA1}$	$1.1V_{DDA1}$	$1.15V_{DDA1}$	V
THD	total harmonic distortion pins 62 and 71 to 75	f_i = 1 kHz; V_i = 1 V (RMS)	–	–71	–61	dB
			–	0.03	0.09	%
$V_{imc(rms)}$	maximum conversion input voltage level pins 62 and 71 to 75 (RMS value)	THD < 1%	1.1	–	–	V
RES	DAC resolution		–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio for DAC and operational amplifiers	R_L > 5 kΩ AC; R_{fb} = 2.7 kΩ; f_i = 1 kHz; R_{ref} = 18 kΩ; V_{oFS} = 2.8 V (p-p); maximum I^2S-bus signal	–	–70	–57	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB; A-weighted	92	102	–	dB
DS	digital silence of DAC	f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dB
$f_{xtalDSP}$	crystal frequency DSP part		–	36.86	–	MHz

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7707H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT318-2

6 BLOCK DIAGRAM

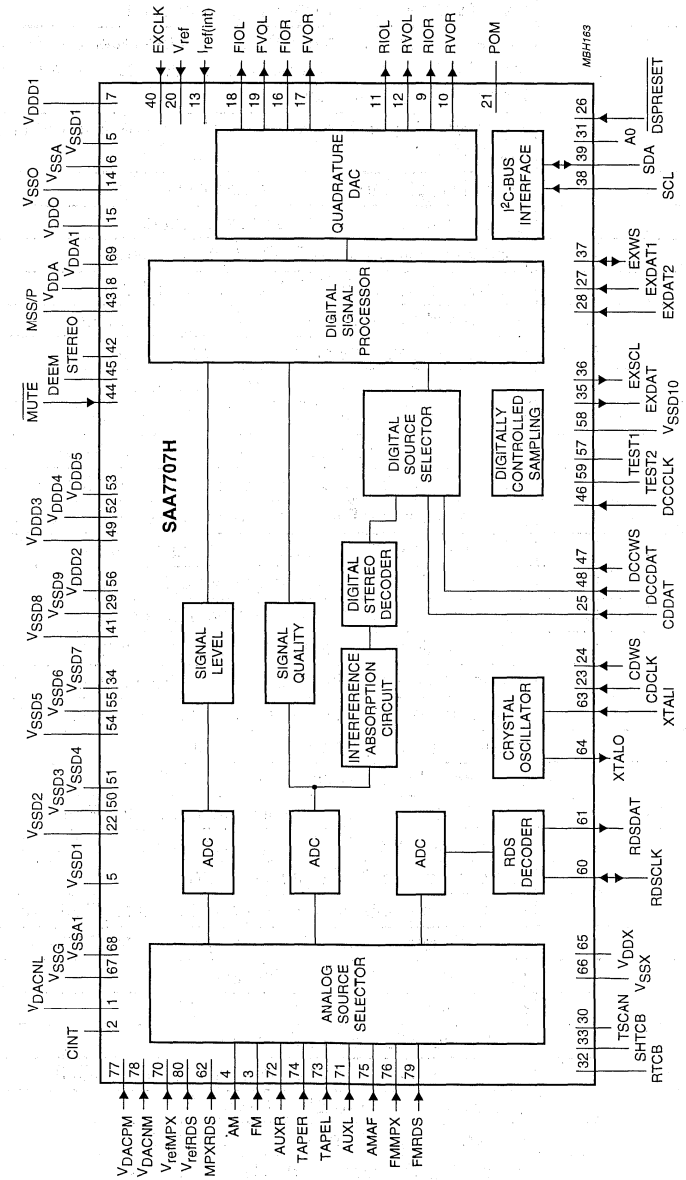


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACNL}	1	–	internal ground reference voltage for the level ADC
CINT	2		level ADC switch-mode integrator connector
FM	3	I	FM level input; via this pin, the level of the received FM radio signal is fed to the CDSP, the level information is required to enable correct functioning of the weak signal behaviour
AM	4	I	AM level input; via this pin, the level of the received AM radio signal is fed to the CDSP
V_{SSD1}	5	–	ground supply 1 for the DACs digital circuitry
V_{SSA}	6	–	ground supply for the DACs analog circuitry
V_{DDD1}	7	–	positive supply 1 for the DACs digital circuitry
V_{DDA}	8	–	positive supply for the DACs analog circuitry
RIOR	9	O	analog audio current output for rear right speaker
RVOR	10	O	analog audio voltage output for rear right speaker
RIOL	11	O	analog audio current output for rear left speaker
RVOL	12	O	analog audio voltage output for rear left speaker
$I_{ref(int)}$	13	I	internal reference current source input for the DACs
V_{SSO}	14	–	ground supply for DAC output operational amplifiers
V_{DDO}	15	–	positive supply for DAC output operational amplifiers
FIOR	16	O	analog audio current output for front right speaker
FVOR	17	O	analog audio voltage output for front right speaker
FIOL	18	O	analog audio current output for front left speaker
FVOL	19	O	analog audio voltage output for front left speaker
V_{ref}	20	I	voltage input for the internal reference buffer amplifier of the DAC
POM	21		activates the Power-on mute; timing is determined with an external capacitor
V_{SSD2}	22	–	ground supply 2 for the digital circuitry
CDCLK	23	I	clock input for CD digital audio source (I^2S-bus)
CDWS	24	I	Word Select input for CD digital audio source (I^2S-bus)
CDDAT	25	I	left/right data input for CD digital audio source (I^2S-bus)
$\overline{\text{DSPRESET}}$	26	I	input to reset DSP core (active LOW)
EXDAT1	27	I	external input data channel 1 (front) from extra DSP chip (I^2S-bus)
EXDAT2	28	I	external input data channel 2 (rear) from extra DSP chip (I^2S-bus)
V_{SSD9}	29	–	ground supply 9 for the digital circuitry
TSCAN	30		scan control (active HIGH)
A0	31		I^2S-bus selection for slave sub-address
RTCB	32		asynchronous reset test control block (active HIGH)
SHTCB	33		shift clock test control block (active HIGH)
V_{SSD7}	34	–	ground supply 7 for the digital circuitry
EXDAT	35	O	output data for extra external DSP chip (I^2S-bus)
EXSCL	36	O	output clock for extra external DSP chip (I^2S-bus)
EXWS	37	I/O	word select input/output for extra external DSP chip (I^2S-bus)

SYMBOL	PIN	I/O	DESCRIPTION
SCL	38	I	serial clock input (I^2C-bus)
SDA	39	I/O	serial data input/output (I^2C-bus)
EXCLK	40	I	external reference clock input to generate $4f_{as}$ and f_{as} synchronization; to be used if the I^2S-bus inputs are not suitable
V_{SSD8}	41	–	ground supply 8 for the digital circuitry
STEREO	42		FM stereo indication (active HIGH)
MSS/P	43		FM pause detector/MSS detector (active HIGH); also for IAC trigger output
$\overline{MUTE}$	44	I	MUTE input pin (active LOW); only for FM mode
DEEM	45		de-emphasis; CD and DCC (active HIGH) (I^2S-bus)
DCCCLK	46	I	DCC digital audio source clock input (I^2S-bus)
DCCWS	47	I	DCC digital audio source Word Select input (I^2S-bus)
DCCDAT	48	I	DCC digital audio source left/right data input (I^2S-bus)
V_{DDD3}	49	–	positive supply 3 for the digital circuitry
V_{SSD3}	50	–	ground supply 3 for the digital circuitry
V_{SSD4}	51	–	ground supply 4 for the digital circuitry
V_{DDD4}	52	–	positive supply 4 for the digital circuitry
V_{DDD5}	53	–	positive supply 5 for the digital circuitry
V_{SSD5}	54	–	ground supply 5 for the digital circuitry
V_{SSD6}	55	–	ground supply 6 for the digital circuitry
V_{DDD2}	56	–	positive supply 2 for the digital circuitry
TEST1	57		test pin 1 (this pin should be left open-circuit)
V_{SSD10}	58	–	ground supply 10 for the digital circuitry
TEST2	59		test pin 2 (this pin should be left open-circuit)
RDSCLK	60	I/O	radio data system bit clock input/output
RDSDAT	61	O	radio data system data output
MPXRDS	62	I	in FM mode, selects between FMMPX and RDSMPX input signal to the MPX decimation filter
XTALI	63	I	crystal oscillator input; can also be used as forced input in slave mode
XTALO	64	O	crystal oscillator output
V_{DDX}	65	–	positive supply crystal circuitry
V_{SSX}	66	–	ground supply crystal circuitry
V_{SSG}	67	–	ground guards for ADCs
V_{SSA1}	68	–	analog ground supply for ADCs
V_{DDA1}	69	–	analog positive supply for ADCs
V_{refMPX}	70	I	common mode reference voltage input for MPX ADC and buffers
AUXL	71	I	analog input for auxiliary left signal
AUXR	72	I	analog input for auxiliary right signal
TAPEL	73	I	analog input for tape left signal
TAPER	74	I	analog input for tape right signal
AMAF	75	I	analog input for AM audio frequency
FMMPX	76	I	analog input for FM multiplex signal

SYMBOL	PIN	I/O	DESCRIPTION
V_{DACPM}	77	I	supply voltage for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
V_{DACNM}	78	I	ground supply for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
FMRDS	79	I	analog FMMPX input for RDS decoding
V_{refRDS}	80	I	common mode reference voltage input for RDS ADC, level ADC and buffers

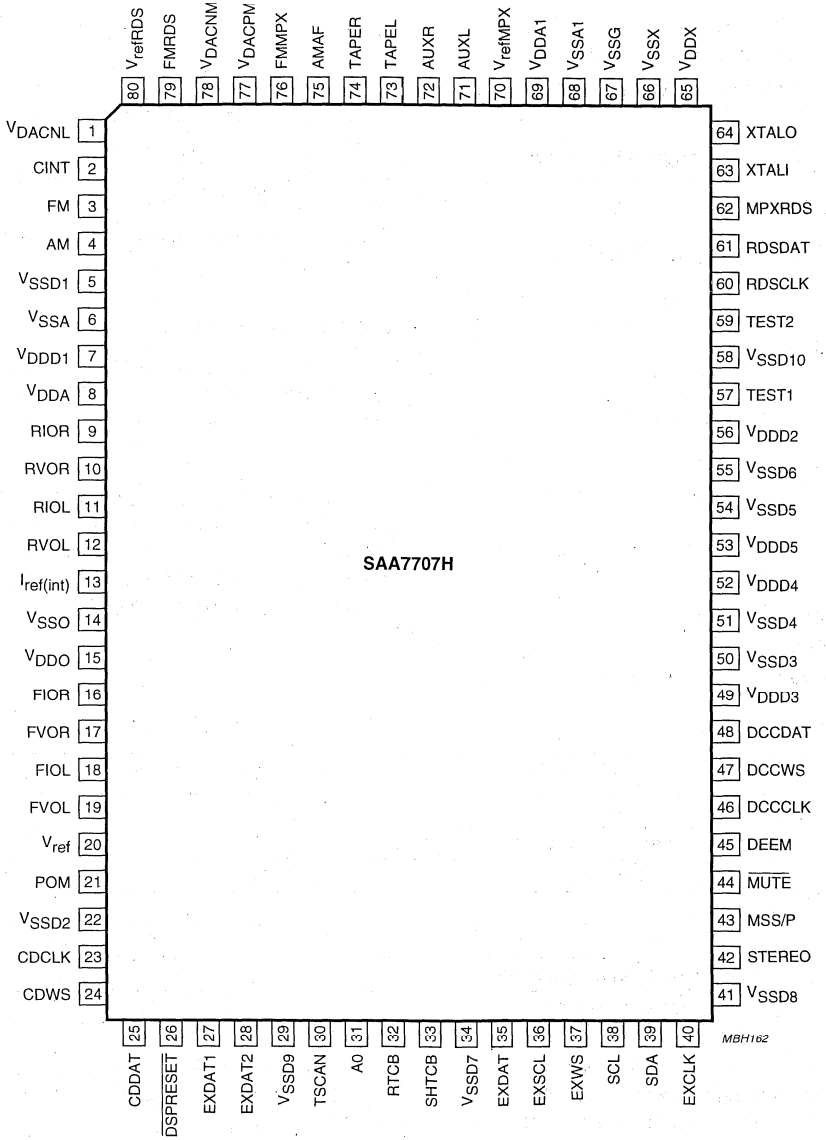


Fig.2 Pin configuration.

Dolby* Pro Logic Surround
Dolby 3 stereo

SAA7710T

FEATURES

- Two stereo I²S-bus digital input channels
- Three stereo I²S-bus digital output channels
- I²C-bus mode control
- Up to 45 ms on-chip delay-line (f_s = 44.1 kHz)
- Optional clock divider for crystal oscillator
- Package: SO32L
- Operating supply voltage range: 4.5 to 5.5 V.

Functions

- 4-channel active surround, 20 Hz to 20 kHz (maximum $f_s/2$)
- Adaptive matrix
- 7 kHz low-pass filters
- Adjustable delay for surround channel
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hall/matrix surround sound functions
- 3-band parametric equalizer on main channels left, centre, right (f_s = 44.1 kHz)
- 5-band parametric equalizer on main channels left, centre, right (f_s = 32 kHz)
- Tone control (bass/treble) on all four output channels (f_s = 44.1 kHz).

GENERAL DESCRIPTION

This datasheet describes the 103 ROM-code version of the SAA7710T chip. The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby surround Pro Logic sound on chip.
In addition to the Dolby surround Pro Logic function, this device also incorporates a 3-band parametric equalizer, a 5-band parametric equalizer, a tone control section and volume control. Instead of Dolby Pro Logic, the surround sound functions can be used together with the equalizer or tone control.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	DC supply voltage	−0.5	–	6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins	–	–	550	mV
V_i	maximum input voltage	−0.5	–	V_{DD} + 0.5	V
I_{DD}	supply current	–	–	50	mA
I_{SS}	supply current	–	–	50	mA
T_{amb}	ambient operating temperature	−40	–	85	°C
T_{stg}	storage temperature range	−65	–	150	°C

Remark Dolby*: Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA94111, USA, from whom licensing and application information must be obtained. "Dolby", the double-D symbol and "Pro Logic" are registered trade-marks of Dolby Laboratories Licensing Corporation.

Dolby* Pro Logic Surround
Dolby 3 stereo

SAA7710T

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7710T/N103	SO32L	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

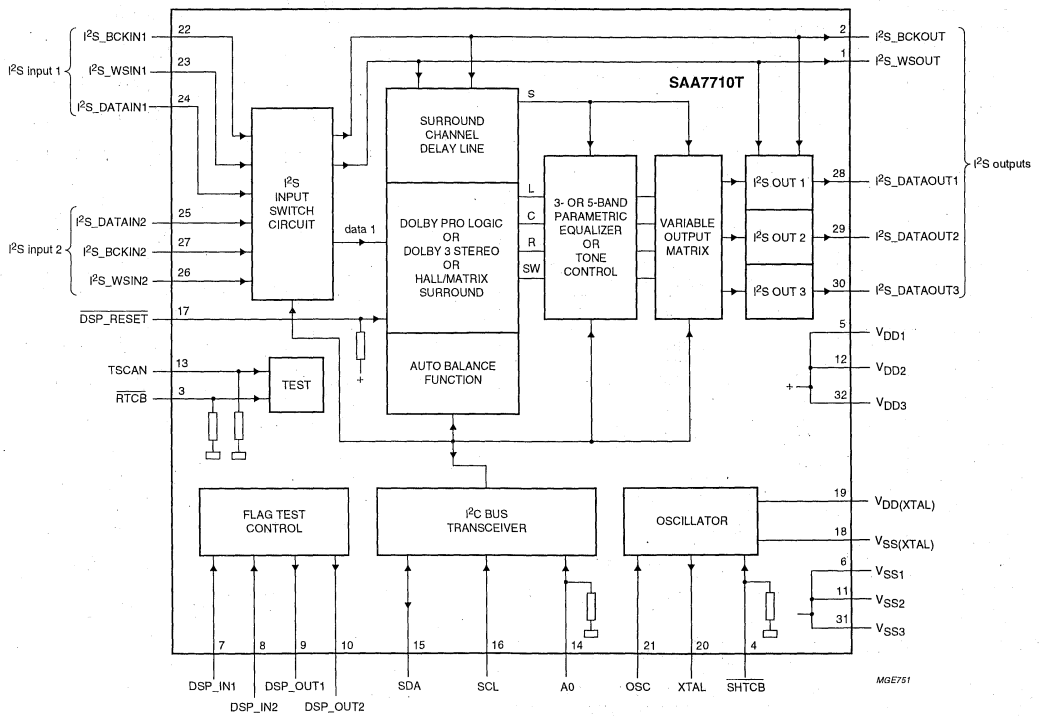


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
I^2S_WSOUT	1	I^2S-bus slave word-select output
I^2S_BCKOUT	2	I^2S-bus slave bit-clock output
$\overline{RTCB}$	3	asynchronous reset test control block input (active low)
$\overline{SHTCB}$	4	clock divider switch enable input (low = divide)
V_{DD1}	5	positive power supply
V_{SS1}	6	ground power supply
DSP_IN1	7	flag input 1
DSP_IN2	8	flag input 2
DSP_OUT1	9	flag output 1
DSP_OUT2	10	flag output 2
V_{SS2}	11	ground power supply
V_{DD2}	12	positive power supply
TSCAN	13	scan control input
A0	14	I^2C-bus slave address selection input
SDA	15	I^2C-bus serial data input/output
SCL	16	I^2C-bus serial clock input
$\overline{DSP\_RESET}$	17	chip reset input (active low)
$V_{SS(XTAL)}$	18	ground power supply crystal oscillator
$V_{DD(XTAL)}$	19	positive power supply crystal oscillator
XTAL	20	crystal oscillator output
OSC	21	crystal oscillator input
I^2S_BCKIN1	22	I^2S-bus master bit-clock input 1
I^2S_WSIN1	23	I^2S-bus master word-select input 1
I^2S_DATAIN1	24	I^2S-bus master data input 1
I^2S_DATAIN2	25	I^2S-bus master data input 2
I^2S_WSIN2	26	I^2S-bus master word-select input 2
I^2S_BCKIN2	27	I^2S-bus master bit-clock input 2
I^2S_DATAOUT1	28	I^2S-bus slave data output 1
I^2S_DATAOUT2	29	I^2S-bus slave data output 2
I^2S_DATAOUT3	30	I^2S-bus slave data output 3
V_{SS3}	31	ground power supply
V_{DD3}	32	positive power supply

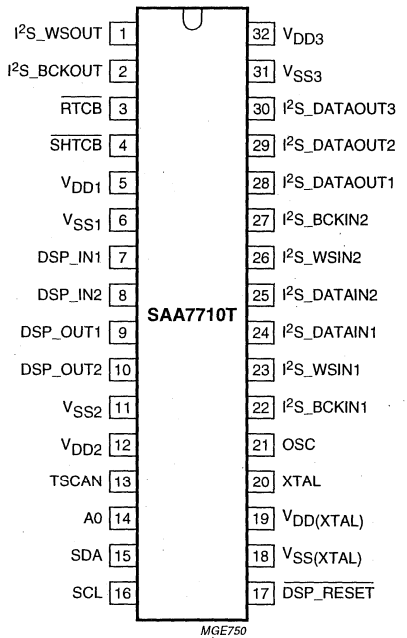


Fig.2 Pin configuration.

Digital Audio Processing IC (DAPIC) SAA7740H

FEATURES

Hardware

- Two digital inputs and two digital outputs in the I²S-bus format (i.e. 4 audio channels)
- Independent input/output interfaces
- Slave input/output interfaces
- Slave processing
- I²C-bus microcontroller interface
- DC filtering at the inputs
- One programmable 2nd-order digital filter unit
- Two multiply accumulate processor units (24 × 16-bit/MAC)
- DRAM interface and address computation unit for external delay lines
- On-chip coefficient and external delay line address storage
- Hardware controlled soft mute via the MUTE pin
- Hardware controlled soft demute via the $\overline{RST}$ pin
- Operating ambient temperature; –40 to +85 °C.

Software

- 5-band parametric equalizer with selectable centre frequency, slope setting and boost/cut gain settings from –12 to +12 dB
- Stereo width control from mono to stereo to spatial stereo
- Stereo Hall-effects for field acoustics, such as concert halls, with 8 coefficients and 8 delayed taps per channel
- External delay line processing for delays up to 1 second
- Reverberation with selectable reverberation time (up to 5 seconds) and energy
- Three different surround sound programs to obtain a spatial effect on 4 loudspeakers
- Passive DOLBY surround processing with the addition of an external dynamic noise reduction IC
- Karaoke processing
- Dual 16th-order correction filtering
- Quad 8th-order correction filtering
- Digital volume and balance control
- Soft controlled soft mute/demute via the microcontroller interface
- Input switching matrix
- Output rear and front switching matrix.

APPLICATIONS

- Digital amplifiers
- Audio combination sets
- Car audio systems
- TV audio channels.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(tot)}$	total DC supply voltage	all V_{DD} pins	4.5	5.0	5.5	V
$I_{DD(tot)}$	total DC supply current	f_{xtal} = 16.9344 MHz	–	60	–	mA
f_{xtal}	input crystal frequency		12.288	16.9344	23.0	MHz
P_{tot}	total power dissipation	f_{xtal} = 16.9344 MHz	–	0.3	–	W
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7740H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

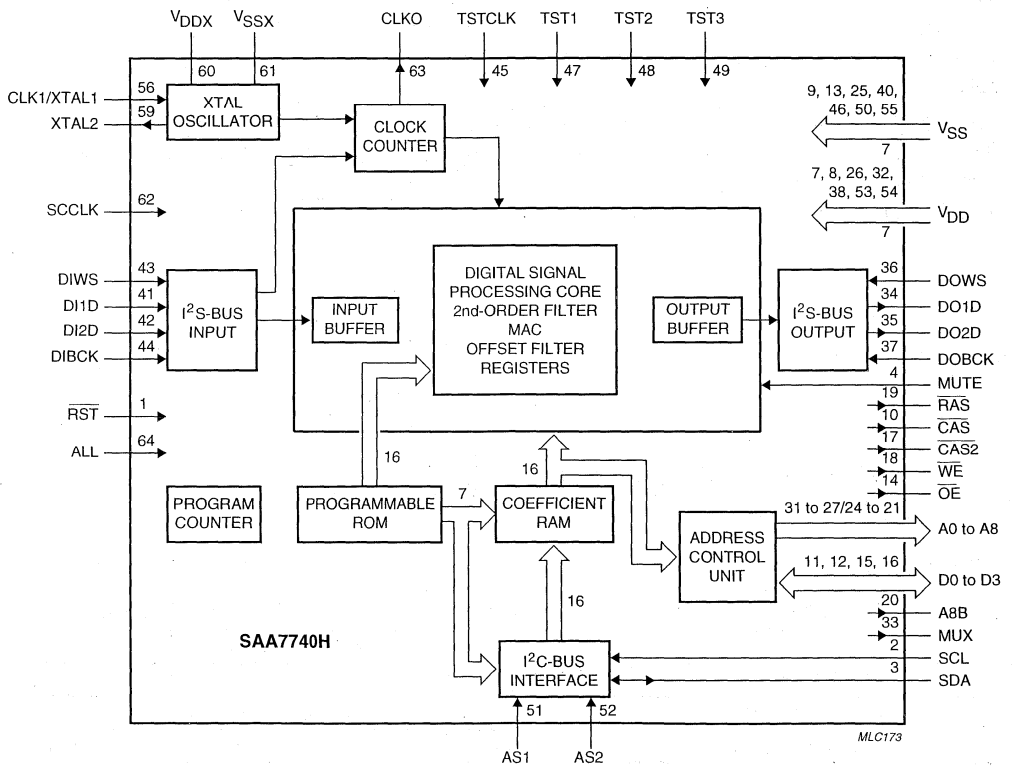


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	1	reset input (active LOW)
SCL	2	serial clock input (I^2C-bus)
SDA	3	serial data input/output (I^2C-bus)
MUTE	4	mute input (active HIGH)
n.c.	5	not connected
n.c.	6	not connected
V_{DD}	7	supply voltage
V_{DD}	8	supply voltage
V_{SS}	9	ground supply
$\overline{CAS}$	10	column address strobe (DRAM) (active LOW)
D0	11	input/output data bus line 0 (DRAM)
D1	12	input/output data bus line 1 (DRAM)
V_{SS}	13	ground supply
$\overline{OE}$	14	output buffer enable (DRAM) (active LOW)
D2	15	input/output data bus line 2 (DRAM)
D3	16	input/output data bus line 3 (DRAM)
$\overline{CAS2}$	17	second column address strobe (active LOW)
$\overline{WE}$	18	write enable (DRAM; active LOW)
$\overline{RAS}$	19	row address strobe (DRAM; active LOW)
A8B	20	inverse MSB address line output (DRAM)
A8	21	address line output 8 (DRAM)
A7	22	address line output 7 (DRAM)
A6	23	address line output 6 (DRAM)
A5	24	address line output 5 (DRAM)
V_{SS}	25	ground supply
V_{DD}	26	supply voltage
A4	27	address line output 4 (DRAM)
A3	28	address line output 3 (DRAM)
A2	29	address line output 2 (DRAM)
A1	30	address line output 1 (DRAM)
A0	31	address line output 0 (DRAM)
V_{DD}	32	supply voltage
MUX	33	address latch strobe output (SRAM)

SYMBOL	PIN	DESCRIPTION
DO1D	34	digital audio output 1 (I^2S-bus)
DO2D	35	digital audio output 2 (I^2S-bus)
DOWS	36	digital audio input word select
DOBCK	37	digital audio input serial bit clock
V_{DD}	38	supply voltage
n.c.	39	not connected
V_{SS}	40	ground supply
DI1D	41	digital audio input 1 (I^2S-bus)
DI2D	42	digital audio input 2 (I^2S-bus)
DIWS	43	digital audio input word select
DIBCK	44	digital audio input serial bit clock
TSTCLK	45	clock input for test mode (should be tied LOW)
V_{SS}	46	ground supply
TST1	47	test pin input 1 (should be tied LOW)
TST2	48	test pin input 2 (should be tied LOW)
TST3	49	test pin input 3 (should be tied LOW)
V_{SS}	50	ground supply
AS1	51	address select input 1 (I^2C-bus)
AS2	52	address select input 2 (I^2C-bus)
V_{DD}	53	supply voltage
V_{DD}	54	supply voltage
V_{SS}	55	ground supply
CLK1/ XTAL1	56	clock or crystal input
n.c.	57	not connected
n.c.	58	not connected
XTAL2	59	crystal output 2
V_{DDX}	60	crystal supply voltage
V_{SSX}	61	crystal ground supply
SCCLK	62	scan test clock input (should be tied LOW)
CLKO	63	clock signal output
ALL	64	mode select input (should be tied HIGH)

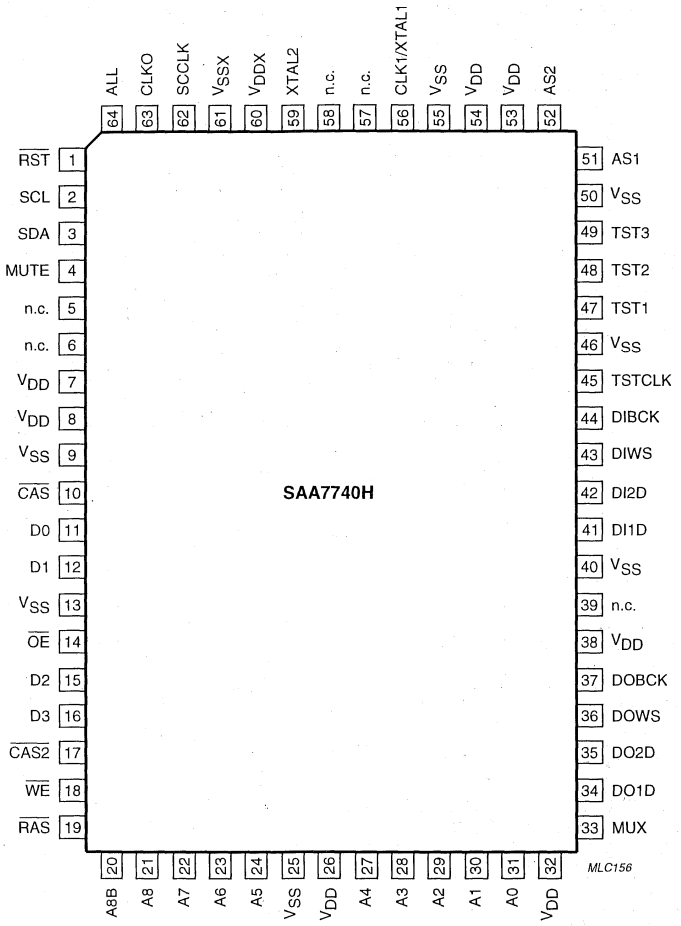


Fig.2 Pinning diagram.

Photodetector amplifiers and laser supply

TDA1300T

FEATURES

- Six input buffer amplifiers with low-pass filtering with virtually no offset
- HF data amplifier with a high or low gain mode
- Two built-in equalizers for single or double speed mode ensuring high playability in both modes
- Full automatic laser control including stabilization and an on/off switch and containing a separate supply V_{DDL} for power reduction
- Applicable with N-sub laser with N-sub or P-sub monitor diode
- Adjustable laser bandwidth and laser switch-on current slope
- Protection circuit preventing laser damage due to supply voltage dip
- Optimized interconnect between pick-up detector and TDA1301
- Wide supply voltage range
- Wide temperature range
- Low-power consumption.

GENERAL DESCRIPTION

The TDA1300 is an integrated data amplifier and laser supply for three beam pick-up detectors applied in a wide range of mechanisms for Compact Disc and Read Only optical systems. It offers 6 amplifiers which amplify and filter the focus and radial diode signals adequately and provides an equalized RF signal for single or double speed mode which can be switched by means of the speed control pin.

The device can handle astigmatic, single foucault and double foucault detectors and is applicable with all N-sub laser, N-sub or P-sub monitor diode units.

After a single initial adjustment the circuit keeps control over the laser diode current resulting in a constant light output power independent of ageing. The chip is mounted in a small SO24 package enabling mounting close to the laser pick-up unit on the sledge.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	–	5.5	V
Diode current amplifiers 6 times						
G_{dn}	amplification		1.43	1.55	1.67	
$I_{os(d)}$	offset current		–	–	100	nA
B	3 dB bandwidth	$I_{i(d)}$ = 1.67 μA	50	–	–	kHz
RFE amplifier (built-in equalizer)						
$t_{d(eq)}$	equalization delay time	f_i = 0.3 MHz	–	320	–	ns
$t_{d(f)}$	flatness delay time	double-speed	–	5	–	ns
Laser supply						
$I_{o(l)}$	output current	V_{DDL} = 3 V	–	–	–100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1300T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

SCHEMATIC DIAGRAM

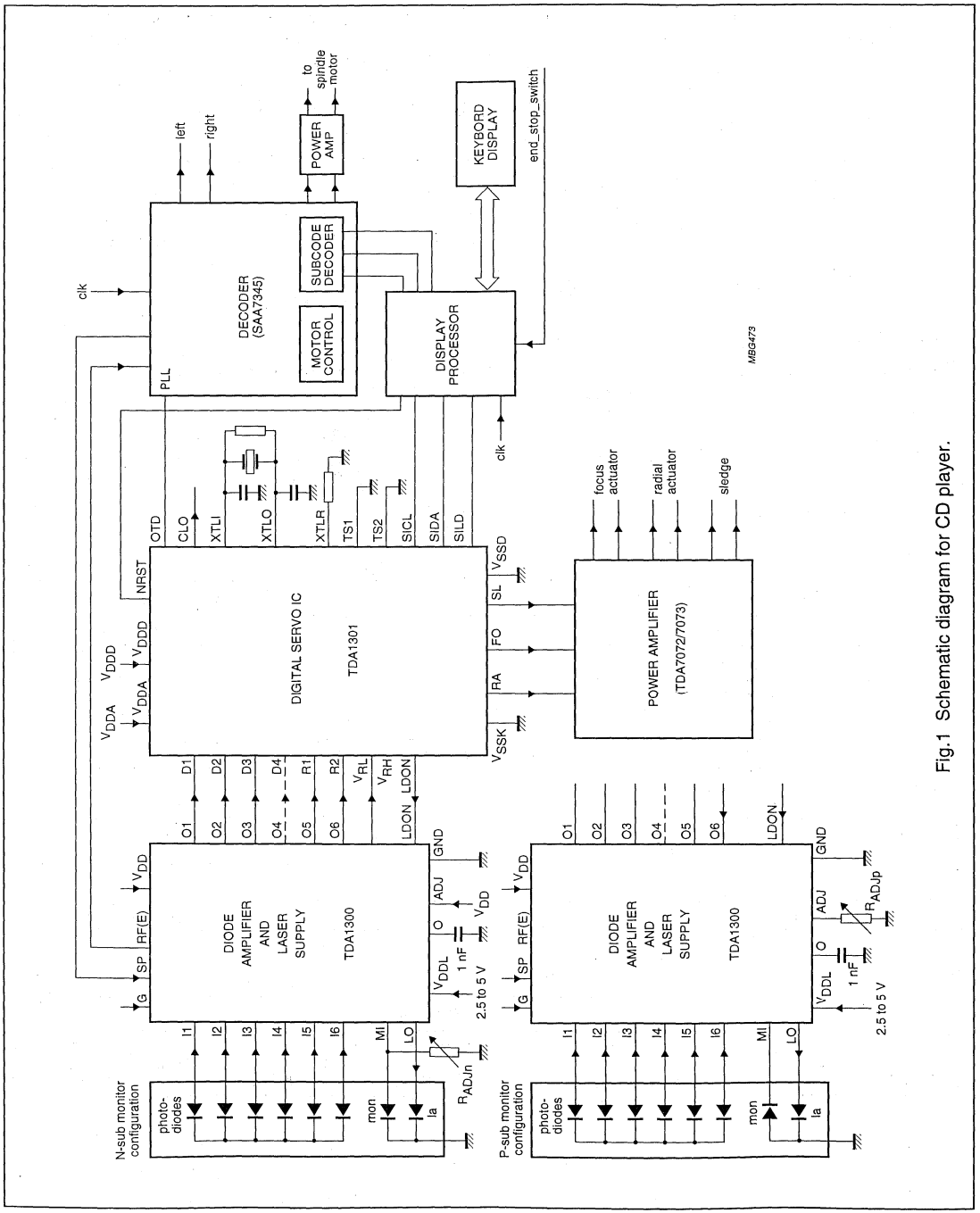


Fig.1 Schematic diagram for CD player.

BLOCK DIAGRAM

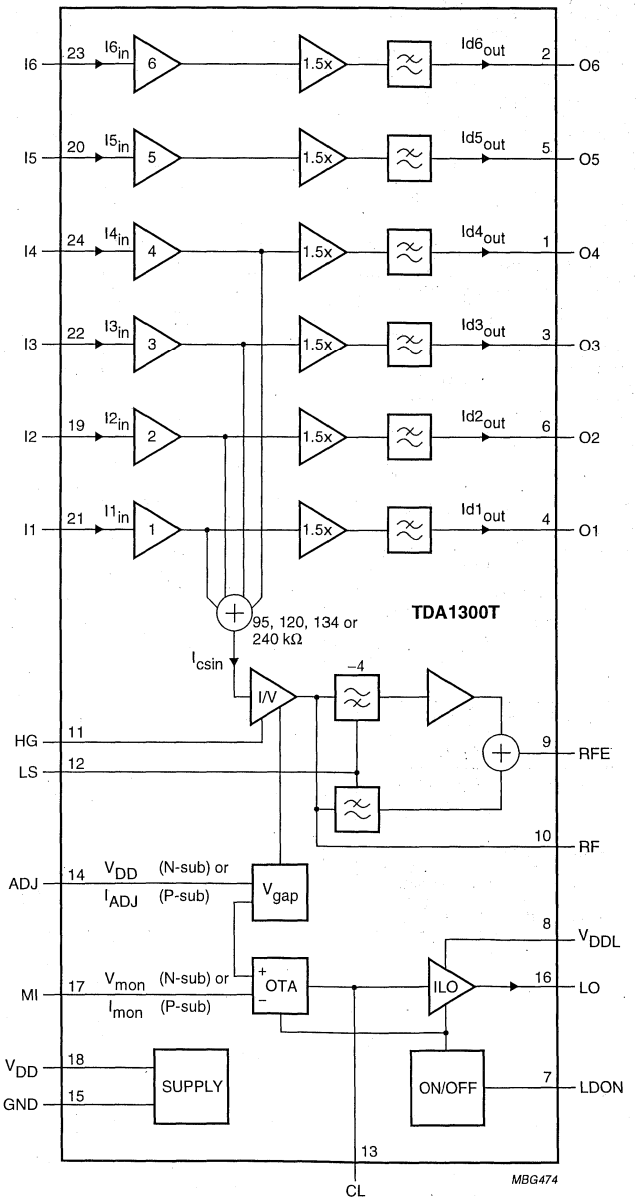


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
O4	1	output of current amplifier 4
O6	2	output of current amplifier 6
O3	3	output of current amplifier 3
O1	4	output of current amplifier 1
O5	5	output of current amplifier 5
O2	6	output of current amplifier 2
LDON	7	control pin for switching the laser on and off
V_{DDL}	8	laser supply voltage
RFE	9	equalized output voltage of sum signal of amplifiers 1 to 4
RF	10	unequalized output
HG	11	control pin for gain switch
LS	12	control pin for speed switch
CL	13	external capacitor
ADJ	14	if connected via resistor to GND P-sub monitor. If connected to V_{DD} N-sub monitor
GND	15	zero supply connection, substrate connection
LO	16	output for the laser, current output
MI	17	input for the monitor diode of the laser
V_{DD}	18	positive supply connection
I2	19	photo detector input 2 (central)
I5	20	photo detector input 5 (satellite)
I1	21	photo detector input 1 (central)
I3	22	photo detector input 3 (central)
I6	23	photo detector input 6 (satellite)
I4	24	photo detector input 4 (central)

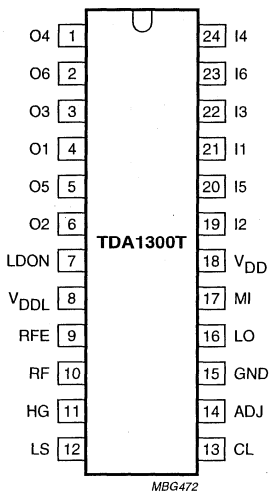


Fig.3 Pin configuration.

Digital servo processor (DSIC2) TDA1301T

FEATURES

The DSIC2 realizes the following servo functions:

- Diode signal preprocessing
- Focus servo loop
- Radial servo loop
- Sledge motor servo loop
- Three-line serial interface via the microcontroller

The other features include:

- Full digital signal processing
- Low power consumption, down to 30 mW
- Low voltage supply 3 to 5.5 V
- Integrated analog-to-digital converters and digital servo loop filters
- Double speed possible
- Easy application
  - Single supply voltage
  - Small number of external components; only 6 decoupling capacitors
  - Flexible system oscillator circuitry
  - Usable for single/double Foucault and astigmatic focus
  - Full automatic radial error signal initialization offset control and level initialization for track position indicator
  - No external adjustments required; no component ageing
  - Wide range of adjustable servo characteristics
  - Simple 3-line serial command interface
  - 28-pin SO package
  - Great flexibility towards different CD mechanisms
  - Full and transparent application information
- High robustness/shock insensitivity
  - Sophisticated track-loss (TL) detection mechanism
  - Fast focus restart procedure
  - Extended radial error signal
  - Adjustable radial shock detector
  - Defect drop-out detector
- Fully automatic jump procedure for radial servo
- Automatic focus start-up procedure and built-in FOK (Focus OK)
- Fast radial jump or access procedure
- Self-operational servo-control without continuous communication via the microcontroller
- Direct communication to photodiode optics; no external preprocessing.

GENERAL DESCRIPTION

The TDA1301T is a fully digital servo processor which has been designed to provide all servo functions, except the spindle motor control, in two-stage three-spot compact disc systems. The device offers a high degree of integration, combined with the low additional cost of external components. The servo characteristics have a wide range of adjustment via a three-line serial interface. This offers an enormous flexibility with respect to applications for different CD mechanisms. The circuit is optimized for low-power low-voltage applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	–	5.5	V
V_{DDA}	analog supply voltage		3.0	–	5.5	V
I_{DDD}	digital supply current		–	5	–	mA
I_{DDA}	analog supply current		–	5	–	mA
$I_{DDD(q)}$	digital quiescent supply current		–	–	10	µA
$I_{i(cd)}$	central diode input currents (D1 to D4)	note 1	–	–	15.8	µA
$I_{i(sd)}$	satellite diode input currents (R1 and R2)	note 1	–	–	7.9	µA
P_{tot}	total power dissipation		–	50	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note

1. f_{sys} = 4.2336 MHz; V_{RL} = 0 V; V_{RH} = 2.5 V (externally applied).

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1301T	28	SO28L	plastic	SOT136A

BLOCK DIAGRAM

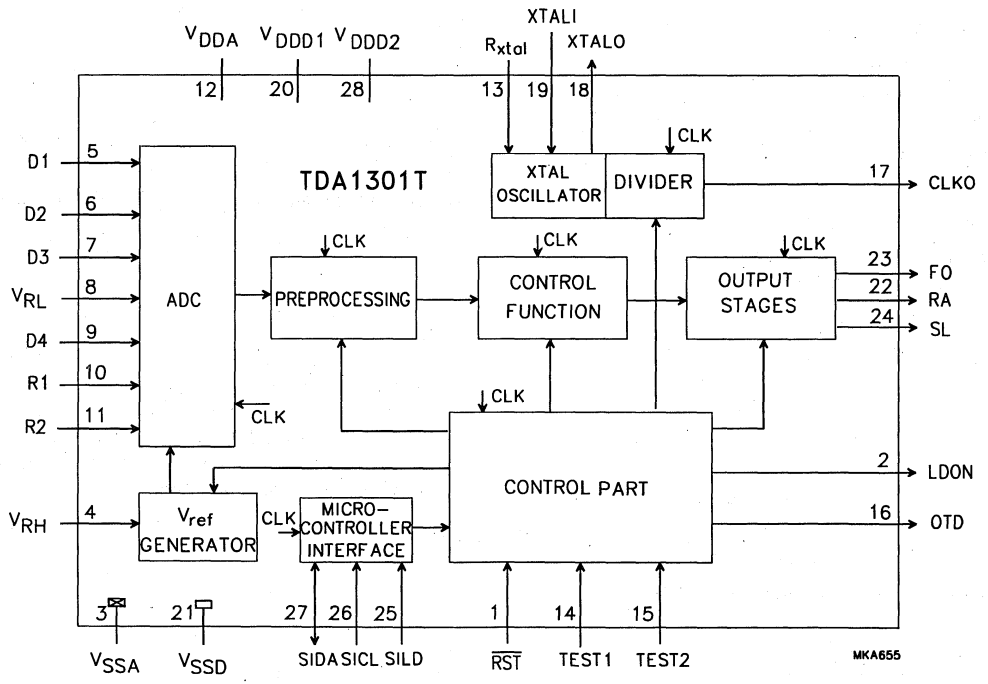


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{RST}$	1	reset input (active LOW)
LDON	2	laser drive on output
V_{SSA}	3	analog ground
V_{RH}	4	reference input for reference voltage generator
D1	5	unipolar current input (central diode signal input)
D2	6	unipolar current input (central diode signal input)
D3	7	unipolar current input (central diode signal input)
V_{RL}	8	reference input for ADC
D4	9	unipolar current input (central diode signal input)
R1	10	unipolar current input (satellite diode signal input)
R2	11	unipolar current input (satellite diode signal input)
V_{DDA}	12	analog supply voltage
$XTAL_{ref}$	13	oscillator reference input
TEST1	14	test input 1
TEST2	15	test input 2
OTD	16	off-track detector output
CLKO	17	clock output
XTALO	18	oscillator output
XTALI	19	oscillator input
V_{DDD1}	20	digital power supply 1
V_{SSD}	21	digital ground
RA	22	radial actuator output
FO	23	focus actuator output
SL	24	sledge output
SILD	25	serial interface load input
SICL	26	serial interface clock input
SIDA	27	serial interface data input/output
V_{DDD2}	28	digital power supply 2

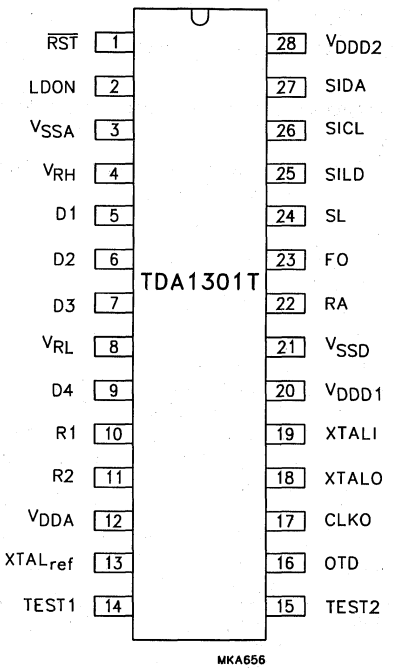


Fig.2 Pin configuration.

Data amplifier and laser supply circuit for CD player and read only optical systems

TDA1302T

FEATURES

- Six input buffer amplifiers with low-pass filtering and with virtually no offset
- HF data amplifier with a high or low gain mode
- Two built-in equalizers for single or double-speed mode ensuring high performance in both modes
- Fully automatic laser control including stabilization and an ON/OFF switch, plus a separate supply (V_{DDL}) for power reduction
- Adjustable laser bandwidth and laser switch-on current slope
- Protection circuit to prevent laser damage due to supply voltage dip
- Optimized interconnectiion between pick-up detector and digital servo processor (TDA1301T)
- Wide supply voltage range
- Wide temperature range
- Low power consumption.

GENERAL DESCRIPTION

The TDA1302T is a data amplifier and laser supply circuit for three-beam pick-up detectors applied in a wide range of mechanisms for Compact Disc and read only optical systems. The device contains 6 amplifiers which amplify and filter the focus and radial diode signals and provides an equalized RF signal suitable for single or double speed mode; the mode can be switched by means of the speed control pin. The device can accommodate astigmatic, single foucault and double foucault detectors and can be applied to all N-sub laser/monitor diode units even though the circuit has been optimized for the Philips CDM12 mechanisms and the digital servo controller TDA1301T. After a single initial adjustment the circuit will maintain control over the laser diode current thus resulting in a constant light output power which is independent of ageing. The IC is mounted in a small-outline package to enable it to be mounted close to the laser pick-up unit on the sledge.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage (pin 18)		3.4	–	5.5	V
Diode current amplifiers						
G_{dn}	amplification		–	1.55	–	dB
$I_{os(d)}$	diode output offset current		–	–	100	nA
B	3 dB bandwidth	$I_{i(d)}$ = 1.67 µA	50	–	–	kHz
RFE amplifier (built-in equalizer)						
$t_{d(eq)}$	equalization delay	f_i = 0.3 MHz	–	320	–	ns
$t_{d(f)}$	flatness delay	double-speed	–	5	–	ns
Laser supply						
$I_{o(l)}$	output current	V_{DDL} = 3 V	–	–	–100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1302T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

SCHEMATIC DIAGRAM

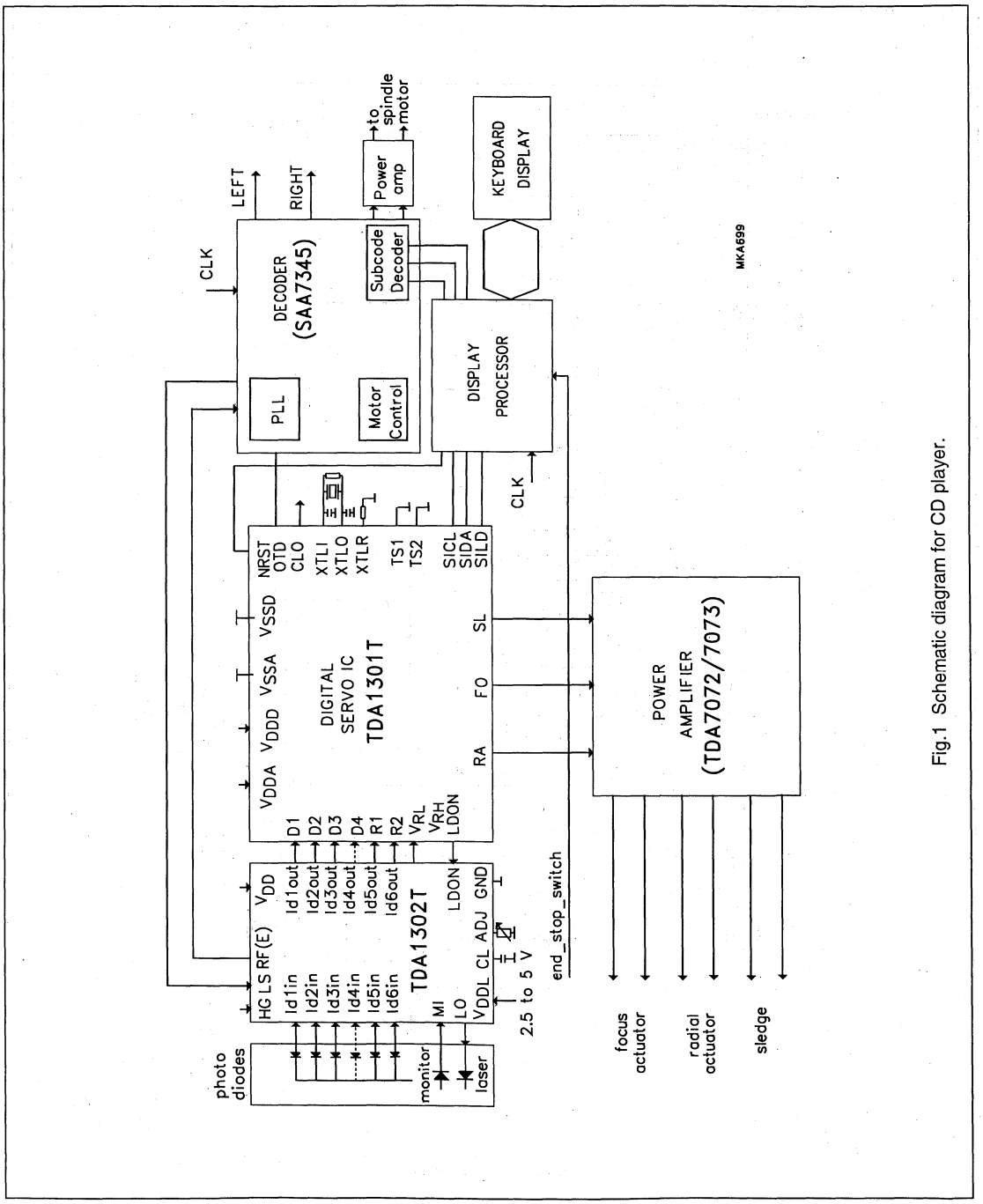


Fig.1 Schematic diagram for CD player.

BLOCK DIAGRAM

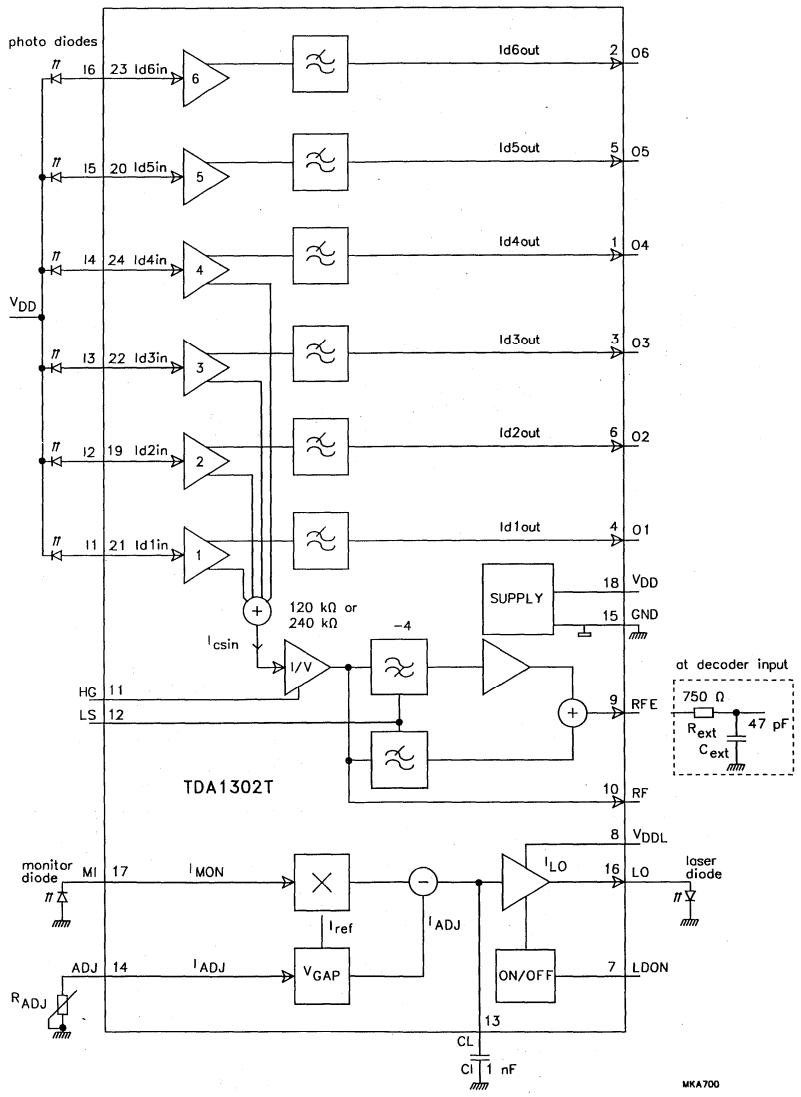


Fig.2 Block diagram.

Data amplifier and laser supply circuit for CD player and read only optical systems

TDA1302T

PINNING

SYMBOL	PIN	DESCRIPTION
O4	1	output of diode current amplifier 4
O6	2	output of diode current amplifier 6
O3	3	output of diode current amplifier 3
O1	4	output of diode current amplifier 1
O5	5	output of diode current amplifier 5
O2	6	output of diode current amplifier 2
LDON	7	control pin for switching the laser ON and OFF
V_{DDL}	8	laser supply voltage
RFE	9	equalized output voltage of sum signal of amplifiers 1 to 4
RF	10	unequalized output
HG	11	control pin for gain switch
LS	12	control pin for speed switch
CL	13	external capacitor
ADJ	14	reference input normally connected to ground via a resistor
GND	15	0 V supply; substrate connection (ground)
LO	16	current output to the laser diode
MI	17	laser monitor diode input
V_{DD}	18	amplifier supply voltage
I2	19	photo detector input 2 (central)
I5	20	photo detector input 5 (satellite)
I1	21	photo detector input 1 (central)
I3	22	photo detector input 3 (central)
I6	23	photo detector input 6 (satellite)
I4	24	photo detector input 4 (central)

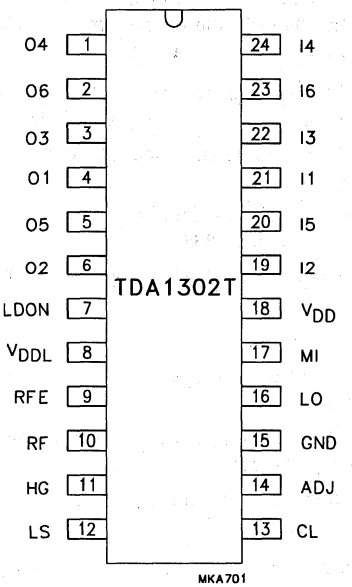


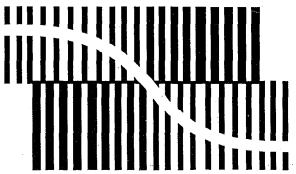
Fig.3 Pin configuration.

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

TDA1305T

FEATURES

- Easy application
- $16f_s$ Finite-duration Impulse-Response (FIR) filter incorporated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus serial input format (at $f_{sys} = 256f_s$) or LSB fixed 16, 18 or 20 bits serial input mode (at $f_{sys} = 384f_s$)
- Slave-mode clock system
- Cascaded 4-stage digital filter incorporating 2-stage FIR filter, linear interpolator and sample-and-hold
- Smoothed transitions before and after muting (soft mute)
- Digital de-emphasis filter for three sampling rates of 32 kHz, 44.1 kHz and 48 kHz
- 12 dB attenuation via the attenuation input control
- Double speed mode
- 2nd order noise shaper
- 96 ($f_{sys} = 384f_s$) or 128 ($f_{sys} = 256f_s$) times oversampling in normal speed mode
- 48 ($f_{sys} = 384f_s$) or 64 ($f_{sys} = 256f_s$) times oversampling in double speed mode
- Bitstream continuous calibration concept
- Small outline SO28 package
- Voltage output 1.5 V (RMS) at line drive level
- Low total harmonic distortion
- No zero crossing distortion
- Inherently monotonic
- No analog post filtering required
- Superior signal-to-noise ratio
- Wide dynamic range (18-bit)
- Single rail supply (3.4 to 5.5 V).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1305T is a new generation of filter-DAC which features a unique combination of bitstream and continuous calibration techniques. The converter functions as a bitstream converter for low signals while large signals are generated using the dynamic continuous calibration technique, thus resulting in low power consumption, small chip size and easy application.

The TDA1305T is a dual CMOS DAC with up-sampling filter and noise shaper. The combination of high oversampling up to $16f_s$, 2nd order noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1305T supports the I^2S-bus data input mode with word lengths of up to 20 bits (at $f_{sys} = 256f_s$) and the LSB fixed serial data input format with word lengths of 16, 18 and 20 bits (at $f_{sys} = 384f_s$). Four cascaded FIR filters increase the oversampling rate to 16 times. A sample-and-hold function increases the oversampling rate to 96 times ($f_{sys} = 384f_s$) or 128 times ($f_{sys} = 256f_s$). A 2nd order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special date coding. This ensures an extremely high signal-to-noise ratio, superior dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage. Externally connected capacitors perform the required 1st order filtering so that no further post filtering is required.

The unique combination of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a single filter-DAC with 18-bit dynamic range, high linearity and simple low cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1305T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.4	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.4	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.4	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	30	–	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	5.5	8	mA
I_{DDO}	operating amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	6.5	9	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V	1.425	1.5	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–81	dB
			–	0.003	0.009	%
		at –60 dB signal level	–	–44	–40	dB
			–	0.63	0.1	%
		at –60 dB signal level; A-weighted	–	–46	–	dB
			–	0.5	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting; at code 00000H	100	108	–	dB
BR_{ns}	input bit rate at data input	f_s = 48 kHz; normal speed	–	–	3.072	Mbits
BR_{ds}	input bit rate at data input	f_s = 48 kHz; double speed	–	–	6.144	Mbits
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. All V_{DD} and V_{SS} pins must be connected to the same supply.

BLOCK DIAGRAM

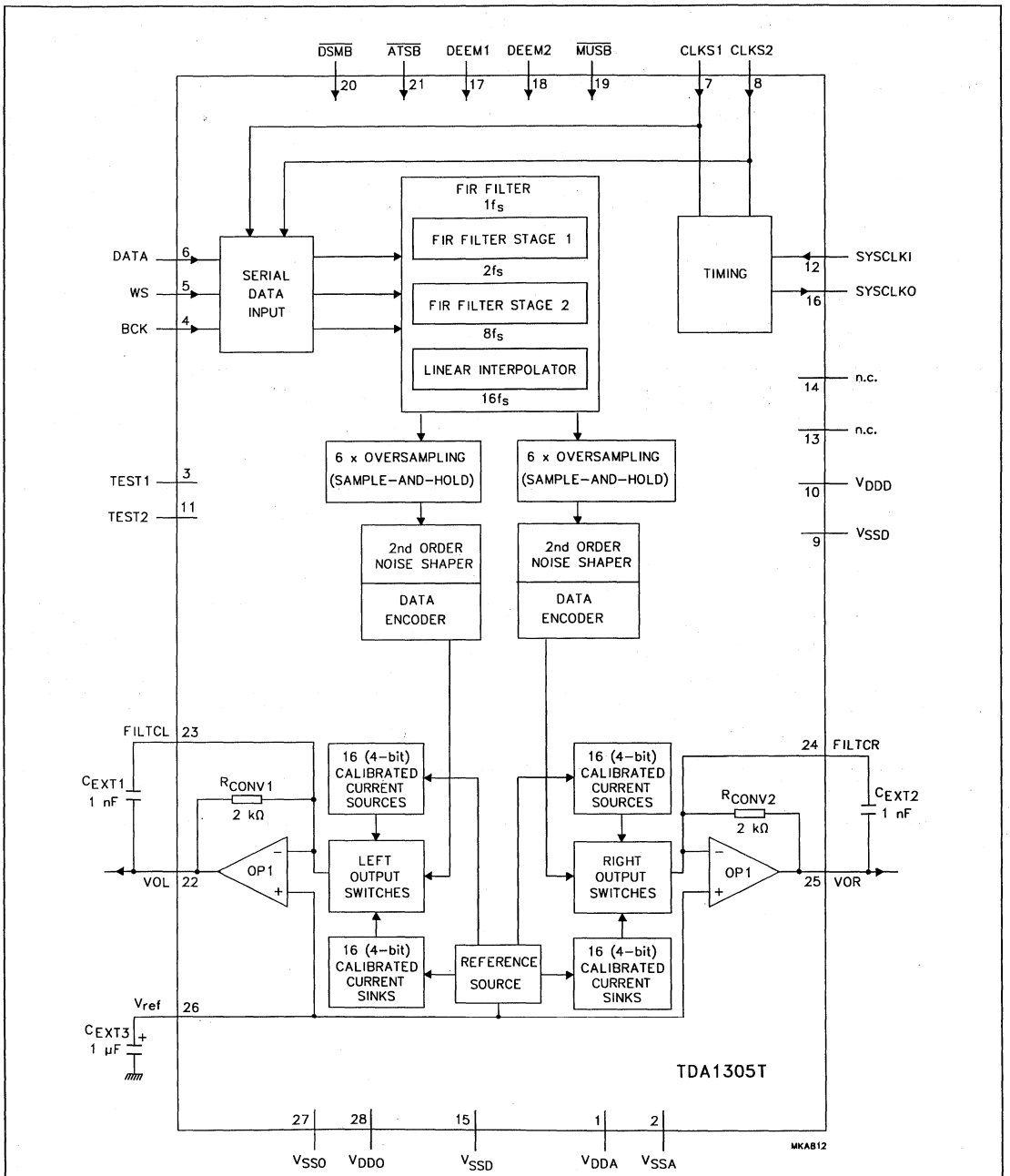


Fig.1 Block diagram.

Stereo 1fs data input up-sampling filter with bitstream continuous dual DAC (BCC-DAC2)

TDA1305T

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
V_{SSA}	2	analog ground
TEST1	3	test input; pin should be connected to ground (internal pull-down resistor)
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock selection 1 input
CLKS2	8	clock selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input; pin should be connected to ground (internal pull-down resistor)
SYSCLKI	12	system clock input
n.c.	13	not connected (this pin should be left open-circuit)
n.c.	14	not connected (this pin should be left open-circuit)
V_{SSD}	15	digital ground
SYSCLKO	16	system clock output
DEEM1	17	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
DEEM2	18	de-emphasis on/off; f_{DEEM} 32 kHz, 44 kHz and 48 kHz
$\overline{MUSB}$	19	mute input (active LOW)
$\overline{DSMB}$	20	double-speed mode input (active LOW)
$\overline{ATSB}$	21	12 dB attenuation input (active LOW)
VOL	22	left channel output
FILTCL	23	capacitor for left channel 1st order filter function should be connected between pins 22 and 23
FILTCR	24	capacitor for right channel 1st order filter function should be connected between pins 25 and 24
VOR	25	right channel output
V_{ref}	26	internal reference voltage for output channels ($0.5V_{DD}$)
V_{SSO}	27	operational amplifier ground
V_{DDO}	28	operational amplifier supply voltage

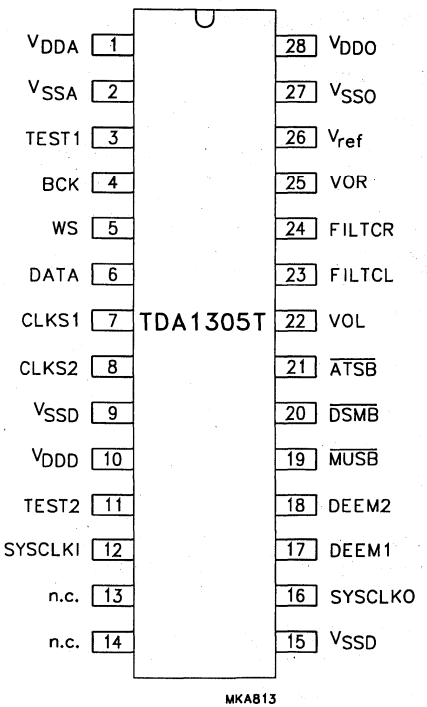


Fig.2 Pin configuration.

Noise shaping filter DAC TDA1306T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis
- TDA1305T pin compatible.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- Selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus ($f_{sys} = 256f_s$) or 16, 18 or 20 bits LSB fixed serial input format ($f_{sys} = 384f_s$).
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1306T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st-order analog post-filtering is required.

The TDA1306T supports the I^2S-bus data input mode ($f_{sys} = 256f_s$) with word lengths of up to 20 bits and the LSB fixed serial data input format ($f_{sys} = 384f_s$) with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1306T	SO24	plastic small outline package; 24 leads; body width 7.5 mm.	SOT137–1

QUICK REFERENCE DATA

All power supply pins V_{DD} and V_{SS} must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_L > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz;	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz;	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	Mbits/s
		f_s = 44.1 kHz; double speed	–	–	5.645	Mbits/s
f_{sys}	system clock frequency (pin 12)		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

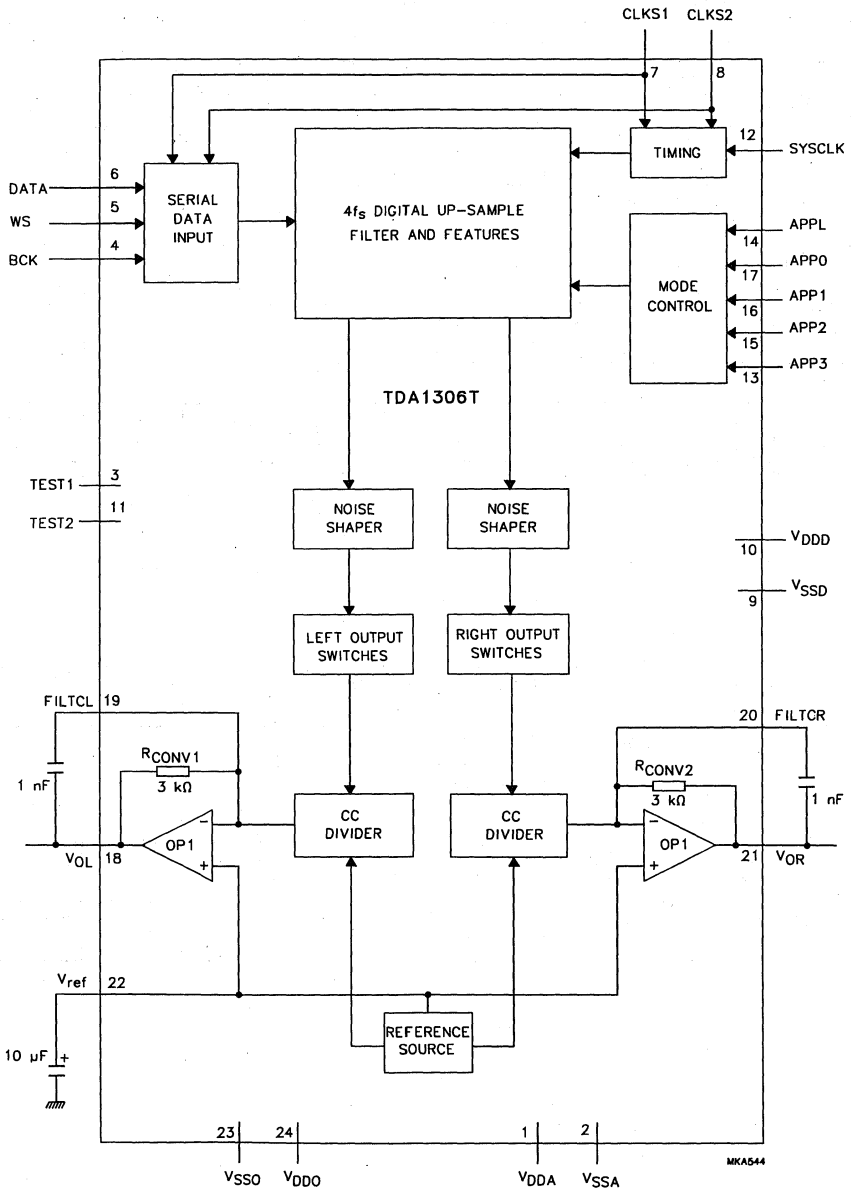


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage (+5 V)
V_{SSA}	2	analog ground
TEST1	3	test input 1; pin should be connected to ground
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CLKS1	7	clock and format selection 1 input
CLKS2	8	clock and format selection 2 input
V_{SSD}	9	digital ground
V_{DDD}	10	digital supply voltage (+5 V)
TEST2	11	test input 2; pin should be connected to ground
SYSCLK	12	system clock input $256f_s$ or $384f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
V_{OL}	18	left channel output
FILTCL	19	capacitor for left channel 1st order filter function; should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st order filter function; should be connected between pins 20 and 21
V_{OR}	21	right channel output
V_{ref}	22	internal reference voltage for output channels; $0.5V_{DDO}$ (typ.)
V_{SSO}	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

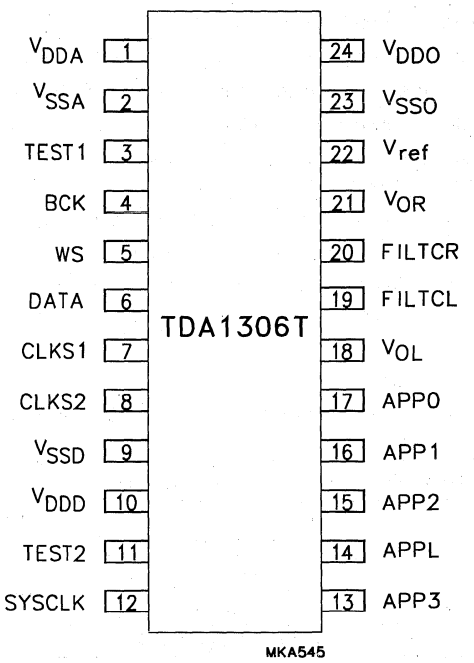
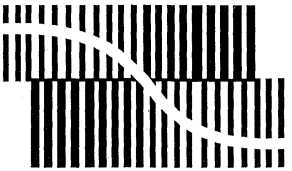


Fig.2 Pin configuration.

High-performance bitstream digital filter TDA1307

FEATURES



BITSTREAM CONVERSION

- Multiple format inputs: I^2S, Sony 16, 18 and 20-bit
- 8-sample interpolation error concealment
- Digital mute, attenuation −12 dB
- Digital audio output function (biphase-mark encoded) according to IEC 958
- Digital silence detection (output)
- Digital de-emphasis (selectable, FS-programmable)
- 8 × oversampling finite impulse response (FIR) filter
- DC-cancelling filter (selectable)
- Peak detection (continuous) and read-out to microprocessor
- Fade function: sophisticated volume control
- Selectable 3rd/4th order noise shaping
- Selectable dither generation and automatic scaling
- Dedicated TDA1547 1-bit output
- Differential mode bitstream: complementary data outputs available
- Simple 3-line serial microprocessor command interface
- Flexible system clock oscillator circuitry
- Power-on reset
- Standby function
- SDIP42 package.

QUICK REFERENCE DATA

Voltages are referenced to V_{SS} (ground = 0 V); all V_{SS} and all V_{DD} connections should be connected externally to the same supply.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDC1,2,3}$	supply voltage (pins 21, 41 and 8)		4.5	5.0	5.5	V
V_{DDOSC}	supply voltage (pin 24)		4.5	5.0	5.5	V
V_{DDAR}	supply voltage (pin 32)		4.5	5.0	5.5	V
V_{DDAL}	supply voltage (pin 29)		4.5	5.0	5.5	V
$I_{DDC1,2,3}$	supply current (pins 21, 41 and 8)	V_{DD} = 5 V	–	75	–	mA
I_{DDOSC}	supply current (pin 24)	V_{DD} = 5 V	–	2	–	mA
I_{DDAR}	supply current (pin 32)	V_{DD} = 5 V	–	2	–	mA
I_{DDAL}	supply current (pin 29)	V_{DD} = 5 V	–	1	–	mA
f_{XTAL}	oscillator clock frequency		–	33.8688	–	MHz
T_{amb}	operating ambient temperature		−20	–	+70	°C
P_{tot}	total power consumption		–	400	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1307	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

GENERAL DESCRIPTION

The TDA1307 is an advanced oversampling digital filter employing bitstream conversion technology, which has been designed for use in premium performance digital audio applications. Audio data is input to the TDA1307 through its multiple-format interface. Any of the four formats (I^2S, Sony 16, 18 or 20-bit) are acceptable. By using a highly accurate audio data processing structure, including 8 times oversampling digital filtering and up to 4th order noise shaping, a high quality bitstream is produced which, when used in the recommended combination with the TDA1547 bitstream DAC, provides the optimum in dynamic range and signal-to-noise performance. With the TDA1307, a high degree of versatility is achieved by a multitude of functional features and their easy accessibility; error concealment functions, audio peak data information and an advanced patented digital fade function are accessible through a simple microprocessor command interface, which also provides access to various integrated system settings and functions.

TDA1307 plus TDA1547 high-performance bitstream digital filter plus DAC combination:

For many features:

- Highly accessible structure
- Intelligent audio data processing.

For optimum performance:

- 4th order noise shaping
- Improvement dynamic range (113 dB)
- Improvement signal-to-noise (115 dB).

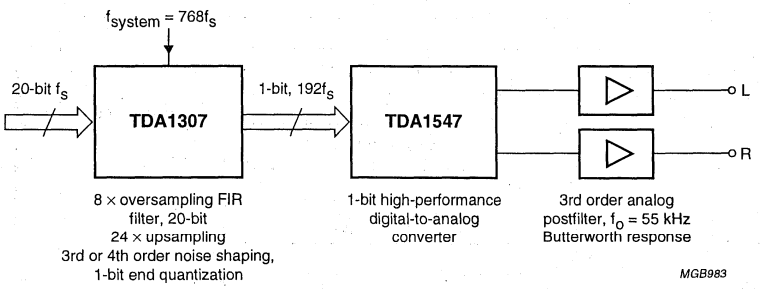


Fig.1 High performance bitstream reconstruction system.

BLOCK DIAGRAM

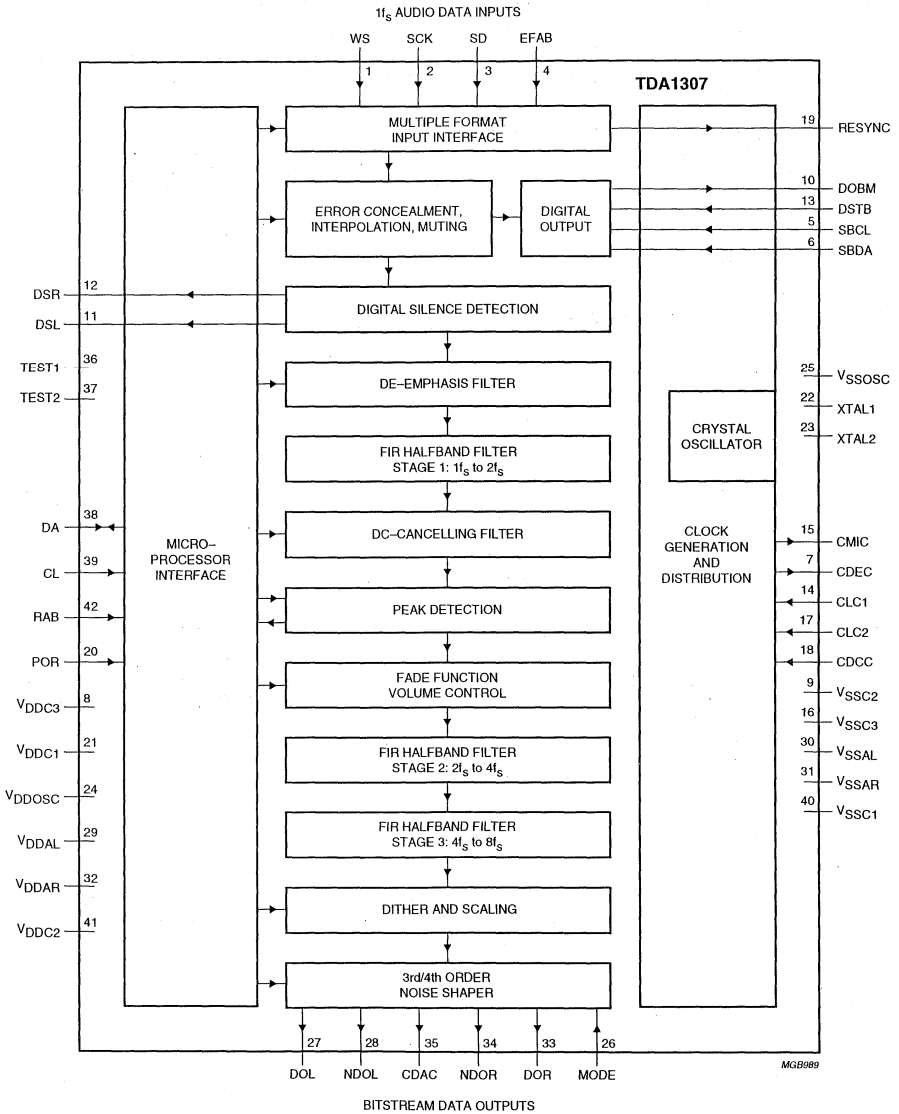


Fig.2 Block diagram.

PINNING

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
WS	1	I	word select input to data interface
SCK	2	I	clock input to data interface
SD	3	I	data input to interface
EFAB	4	I[1]	error flag (active HIGH): input from decoder chip indicating unreliable data
SBCL	5	I	subcode clock: a 10-bit burst clock (typ. 2.8224 MHz) input which synchronizes the subcode data
SBDA	6	I	subcode data: a 10-bit burst of data, including flags and sync bits, serially input once per frame, clocked by burst clock input SBCL
CDEC	7	O	decoder clock output: frequency division programmable by means of pins 14 (CLC1) and 17 (CLC2) to output 192, 256, 384 or 768 times f_s
V_{DDC3}	8		positive supply 3
V_{SSC2}	9		ground 2
DOBM	10	O	digital audio output: this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data; transmission is in biphase-mark code
DSL	11	O	digital silence detected (active LOW) on left channel
DSR	12	O	digital silence detected (active LOW) on right channel
DSTB	13	I[2]	DOBM standby mode enforce pin (active HIGH)
CLC1	14	I	application mode programming pin for CDEC (pin 7) frequency division
CMIC	15	O	clock output, provided to be used as running clock by microprocessor (in master mode only), output $96f_s$
V_{SSC3}	16		ground 3
CLC2	17	I	application mode programming pin for CDEC (pin 7) frequency division
CDCC	18	I	master / slave mode selection pin
RESYNC	19	O	resynchronization: out-of-lock indication from data input section (active HIGH)
POR	20	I[2]	power-on reset (active LOW)
V_{DDC1}	21		supply voltage 1
XTAL1	22	I	crystal oscillator terminal: local crystal oscillator sense forced input in slave mode
XTAL2	23	O	crystal oscillator output: drive output to crystal
V_{DDOSC}	24		positive supply connection to crystal oscillator circuitry
V_{SSOSC}	25		ground connection to crystal oscillator circuitry
MODE	26	I[2]	evaluation mode programming pin (active LOW); in normal operation, this pin should be left open-circuit or connected to the positive supply
DOL	27	O	data output left channel to bitstream DAC TDA1547
NDOL	28	O	complementary data output left channel to TDA1547 in double differential mode
V_{DDAL}	29		positive supply connection to output data driving circuitry, left channel
V_{SSAL}	30		ground connection to output data driving circuitry, left channel
V_{SSAR}	31		ground connection to output data driving circuitry, right channel
V_{DDAR}	32		positive supply connection to output data driving circuitry, right channel
DOR	33	O	data output right channel to TDA1547

SYMBOL	PIN	TYPE, I/O	DESCRIPTION
NDOR	34	O	complementary data output right channel to TDA1547 in double differential mode
CDAC	35	O	clock output to bitstream DAC TDA1547
TEST1	36	I[1]	test mode input; in normal operation this pin should be connected to ground
TEST2	37	I[1]	test mode input; in normal operation this pin should be connected to ground
DA	38	I/O[2]	bidirectional data line intended for control data from the microprocessor and peak data from the TDA1307
CL	39	I[2]	clock input, to be generated by the microprocessor
V_{SSC1}	40		ground 1
V_{DDC2}	41		supply voltage 2
RAB	42	I[2]	command / peak data request line

Notes

1. These pins are configured as internal pull-down.
2. These pins are configured as internal pull-up.

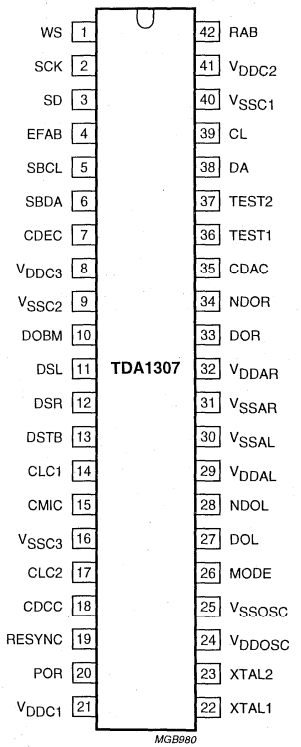


Fig.3 Pin configuration.

Class AB stereo headphone driver TDA1308

FEATURES

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
  - high signal-to-noise ratio
  - high slew rate
  - low distortion
- Large output voltage swing.

GENERAL DESCRIPTION

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

QUICK REFERENCE DATA

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_i = 1 kHz; R_L = 32 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage					
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
P_o	maximum output power	THD < 0.1%; note 1	–	60	–	mW
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 1				
			–	0.03	0.06	%
			–	−70	−65	dB
		R_L = 5 kΩ	–	−101	–	dB
S/N	signal-to-noise ratio		100	110	–	dB
α_{cs}	channel separation		–	70	–	dB
		R_L = 5 kΩ	–	105	–	dB
PSRR	power supply ripple rejection	f_i = 100 Hz; $V_{ripple(p-p)}$ = 100 mV	–	90	–	dB
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. V_{DD} = 5 V; $V_{O(p-p)}$ = 3.5 V (at 0 dB).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1308	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1308T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

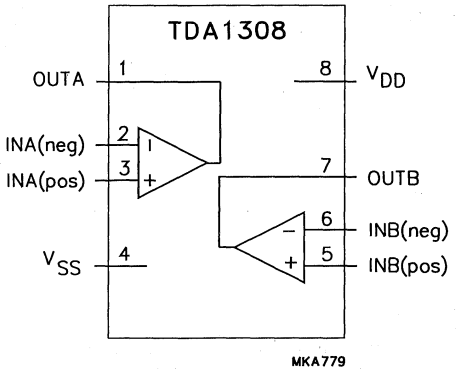


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
V_{DD}	8	positive supply

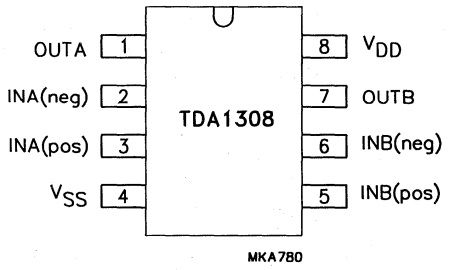


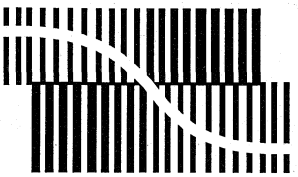
Fig.2 Pin configuration.

Low-voltage low-power stereo bitstream ADC/DAC

TDA1309H

FEATURES

- Low power
- Low supply voltage (2.7 V)
- Integrated high-pass filter to cancel DC offset (ADC)
- Analog loop-through function
- Multiple digital input/output formats possible
- $256f_s$ system clock frequency
- Several power-down modes
- Digital de-emphasis (DAC)
- Overload detector to enable automatic recording level adjustment (ADC)
- Input pads suitable for 5.5 V; low supply voltage interfacing
- High dynamic range
- DAC requires only one capacitor for post-filtering
- Small 44-pin quad flat pack with 0.8 mm pitch
- $256f_s$ system clock frequency in Analog-to-Digital (AD) and Digital-to-Analog (DA) mode
- Choice of three system clock frequencies ($192f_s$, $256f_s$ or $384f_s$) in DA mode.



BITSTREAM CONVERSION

APPLICATION

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1309H is a single chip stereo analog-to-digital and digital-to-analog converter employing bitstream conversion techniques. The low voltage requirement makes the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording and playback functions.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1309H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

$V_{DDD} = V_{DDA} = V_{DDO} = V_{DDD(F)} = 3$ V; $V_{SSD} = V_{SSA} = V_{SSO} = V_{SSD(F)} = 0$ V; $T_{amb} = 25$ °C; full scale sine wave input; mode 1; $f_i = 1$ kHz; 16-bit input data; conversion rate = 44.1 kHz; measurement bandwidth = 10 Hz to 20 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DDA(AD)}$	ADC analog supply voltage (pin 8)		2.7	3.0	4.0	V
$V_{DDA(DA)}$	DAC analog supply voltage (pin 25)		2.7	3.0	4.0	V
V_{DDO}	operational amplifiers supply voltage (pin 19)		2.7	3.0	4.0	V
V_{DDD}	ADC and DAC digital supply voltage (pin 28)		2.7	3.0	4.0	V
$V_{DDD(F)}$	digital filters supply voltage (pin 34)		2.7	3.0	4.0	V
$I_{DDA(AD)}$	ADC analog supply current (pin 8)		–	8	12.5	mA
$I_{DDA(DA)}$	DAC analog supply current (pin 25)		–	3.5	7	mA
I_{DDO}	operational amplifiers supply current (pin 19)		–	12	18	mA
I_{DDD}	ADC and DAC digital supply current (pin 28)		–	0.2	0.5	mA
$I_{DDD(F)}$	digital filters supply current (pin 34)		–	20	30	mA
$I_{PD(DA)}$	DAC power-down current		–	15	20	mA
$I_{PD(AD)}$	ADC power-down current		–	7	10	mA
T_{amb}	operating ambient temperature		–20	–	+75	°C
Analog-to-digital converter						
$V_{I(rms)}$	input voltage (RMS value)	note 1	–	0.5	0.54	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–35	–30	dB
S/N	idle channel signal-to-noise ratio	$V_I = 0$ V; A-weighted	90	95	–	dB
α_{cs}	channel separation		–	90	–	dB
Digital-to-analog converter						
$V_{O(rms)}$	output voltage (RMS value)	note 2	0.43	0.5	0.57	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–90	–82	dB
		at –60 dB; A-weighted	–	–38	–34	dB
		at –60 dB; A-weighted; note 3	–	–44	–	dB
S/N	idle channel signal-to-noise ratio	code 0000H; A-weighted	–	104	–	dB
α_{cs}	channel separation		90	100	–	dB

Notes

1. The input voltage for full scale digital output is a function of $V_{DDA(AD)}$.
2. At full scale digital input; no de-emphasis; $V_{O(rms)}$ is a function of $V_{DDA(DA)}$.
3. 18-bit input data.

BLOCK DIAGRAM

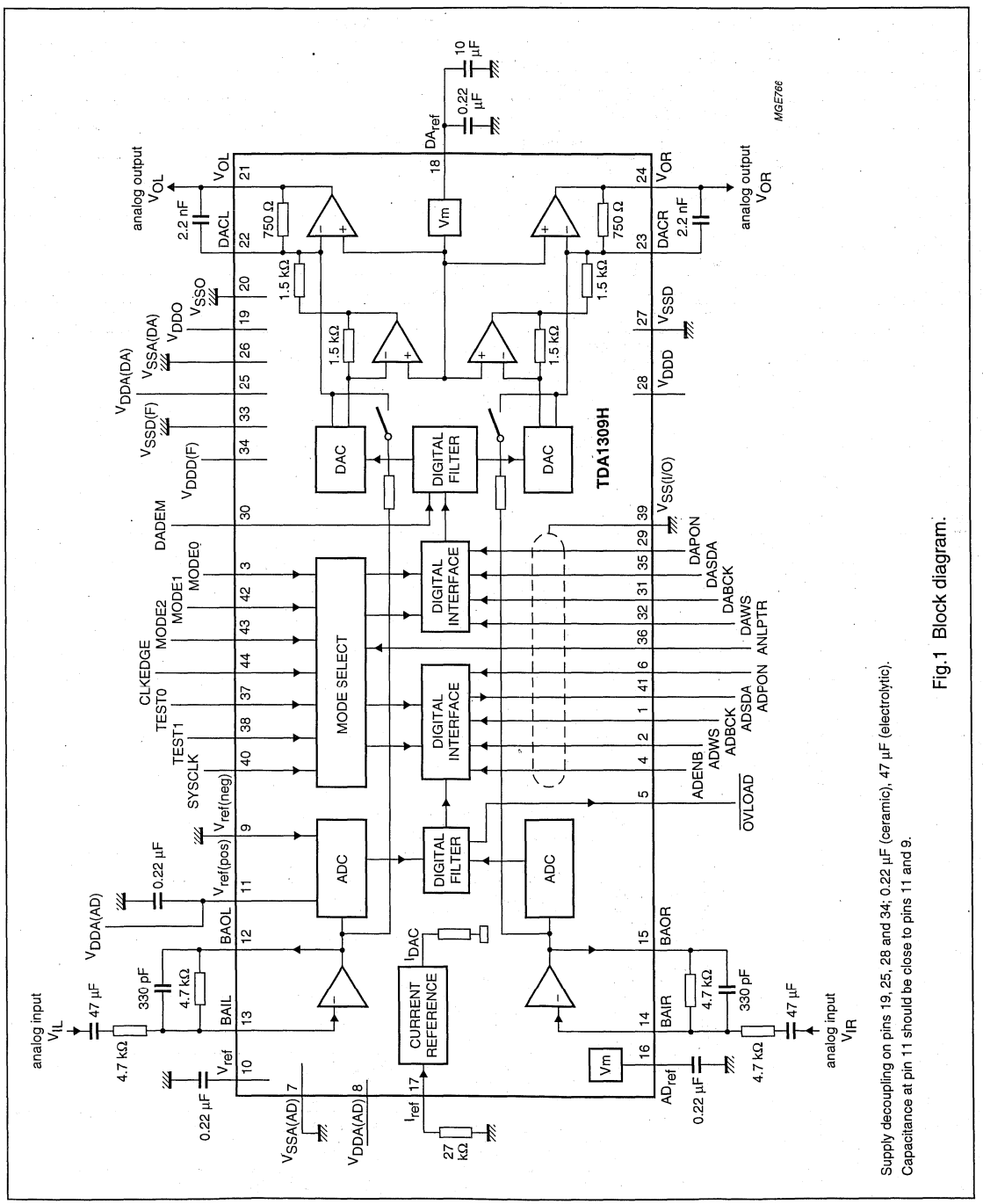


Fig.1 Block diagram.

Supply decoupling on pins 19, 25, 28 and 34; 0.22 µF (ceramic), 47 µF (electrolytic).
Capacitance at pin 11 should be close to pins 11 and 9.

PINNING

SYMBOL	PIN	DESCRIPTION
ADBCK	1	ADC input bit clock; $32f_s$ or $64f_s$
ADWS	2	ADC word select input at f_s
MODE0	3	ADC/DAC mode select input
ADENB	4	ADC serial data enable input (active HIGH)
$\overline{OVLOAD}$	5	ADC output overload flag (active LOW)
ADPON	6	ADC power-on-mode input (active HIGH)
$V_{SSA(AD)}$	7	ADC analog ground supply voltage
$V_{DDA(AD)}$	8	ADC analog supply voltage
$V_{ref(neg)}$	9	ADC negative reference voltage input (ground)
V_{ref}	10	ADC decoupling capacitor
$V_{ref(pos)}$	11	ADC positive reference voltage decoupling capacitor
BAOL	12	ADC input amplifier output left
BAIL	13	ADC input amplifier virtual ground left
BAIR	14	ADC input amplifier virtual ground right
BAOR	15	ADC input amplifier output right
AD_{ref}	16	ADC decoupling capacitor
I_{ref}	17	ADC/DAC reference current resistor input
DA_{ref}	18	DAC decoupling capacitor
V_{DDO}	19	ADC/DAC operational amplifier supply voltage
V_{SSO}	20	ADC/DAC operational amplifier ground supply voltage
V_{OL}	21	DAC output voltage left
DACL	22	DAC output current left
DACR	23	DAC output current right
V_{OR}	24	DAC output voltage right
$V_{DDA(DA)}$	25	DAC analog supply voltage
$V_{SSA(DA)}$	26	DAC analog ground supply voltage
V_{SSD}	27	ADC/DAC digital ground supply voltage
V_{DDD}	28	ADC/DAC digital supply voltage
DAPON	29	DAC power-on-mode input (active HIGH)
DADEM	30	DAC digital de-emphasis input (active HIGH)
DABCK	31	DAC input bit clock; $32f_s$, $48f_s$ or $64f_s$
DAWS	32	DAC word select input at f_s
$V_{SSD(F)}$	33	ADC/DAC digital filters ground supply voltage
$V_{DDD(F)}$	34	ADC/DAC digital filters supply voltage
DASDA	35	DAC serial data input
ANLPTR	36	ADC/DAC analog loop-through input (active HIGH)
TEST0	37	ADC/DAC enable test mode 0 input (LOW is normal mode)
TEST1	38	ADC/DAC enable test mode 1 input (LOW is normal mode)
$V_{SS(I/O)}$	39	ADC/DAC digital input/output ground supply voltage
SYSCLK	40	ADC/DAC system clock input ($f_{sys} = 256f_s$; DAC also $192f_s$ and $384f_s$)

SYMBOL	PIN	DESCRIPTION
ADSDA	41	ADC serial data output
MODE1	42	ADC/DAC mode 1 select input
MODE2	43	ADC/DAC mode 2 select input
CLKEDGE	44	ADC/DAC input bit clock rising/falling edge

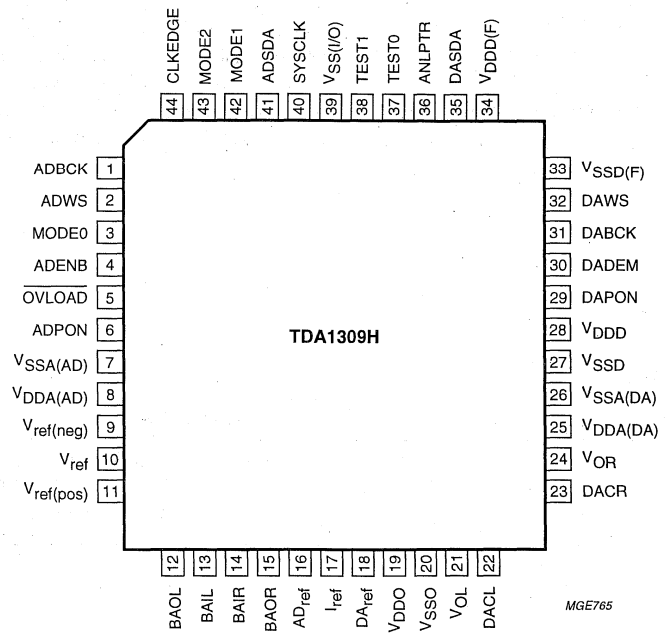


Fig.2 Pin configuration.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1310A

FEATURES

- Space saving package DIL8 or SO8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - Single 3 to 5 V supply rail
  - Output current and bias current are proportional to the supply voltage
- Fast settling time permits 2×, 4× and 8× oversampling (serial input) or double speed operation at 4× oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (-40 t +85 °C)
- Compatible with most current Japanese input formats:
  - Time multiplexed
  - Two's complement
  - TTL
- No zero-crossing distortion.

GENERAL DESCRIPTION

The TDA1310A is a device of a new generation of Digital-to-Analog Converters (DACs) which embodies the innovative technique of Continuous Calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The TDA1310A is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method precludes zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1310A	8	DIL8	plastic	SOT97DE
TDA1310AT	8	SO8	plastic	SOT96AG

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.9	1.0	1.1	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–65	–61	dB
			–	0.05	0.08	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2.2	–	%
		at –60 dB signal level; A-weighted; R3 = R4 = 11 kΩ; (see Fig.1); I_{FS} = 2 mA	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
		A-weighted; I_{FS} = 2 mA; R3 = R4 = 11 kΩ; see Fig.1	–	95	–	dB
t_{CS}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{clk}	clock frequency at clock input BCK		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	15	20	mW
		V_{DD} = 3 V at code 0000H	–	6.0	–	mW

BLOCK DIAGRAM

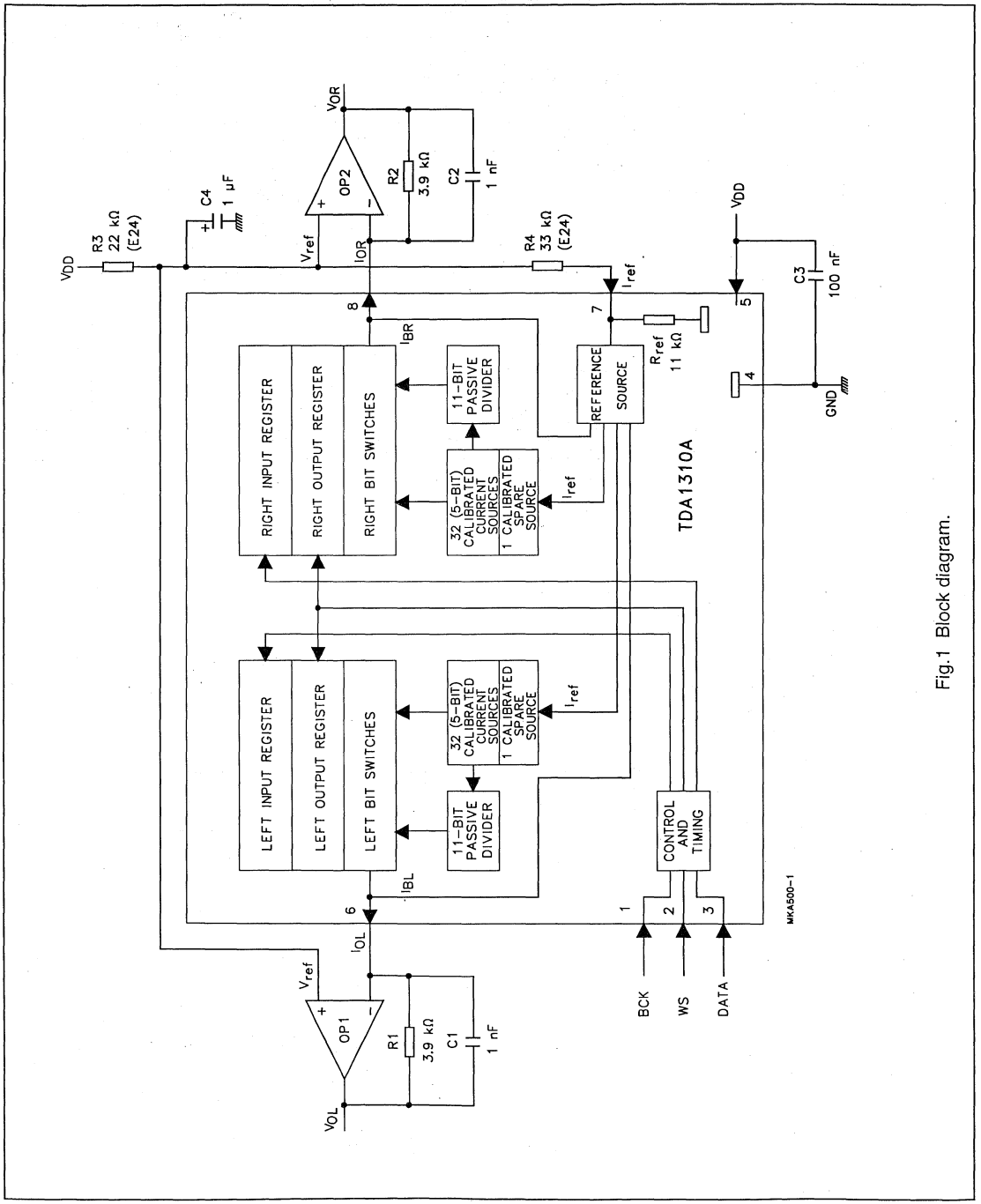


Fig.1 Block diagram.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1310A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
I_{OL}	6	left channel output
I_{ref}	7	reference input
I_{OR}	8	right channel output

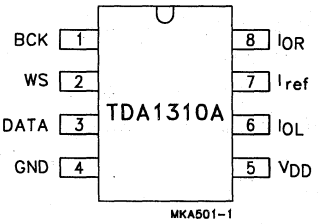


Fig.2 Pin configuration.

Stereo Continuous Calibration DAC (CC-DAC)

TDA1311A

FEATURES

- Voltage output
- Space saving packages SO8 or DIP8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
  - single 4 to 5.5 V rail supply
  - output current and bias current are proportional to the supply voltage
  - integrated current-to-voltage converter
- Fast settling time permits 2, 4 and 8 × oversampling (serial input) or double-speed operation at 4 × oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 °C to +85 °C)
- Compatible with most current Japanese input formats: time multiplexed, two's complement, TTL
- No zero-crossing distortion
- Cost efficient.

GENERAL DESCRIPTION

The TDA1311A; AT is a voltage-driven digital-to-analog converter and is new generation of DAC devices which embodies the innovative technique of Continuous Calibration (CC). The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle which has an accuracy insensitive to ageing, temperature matching and process variations.

The TDA1311A; AT is fabricated in a 1.0 μm CMOS process and features an extremely low-power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1311A	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1311AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	3.4	6.0	mA
V_{FS}	full scale output voltage	V_{DD} = 5 V	1.8	2.0	2.2	V
(THD+N)/S	total harmonic distortion plus noise	at 0 dB signal level	–	–68	–63	dB
			–	0.04	0.07	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		–	±400	–	ppm
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	17	30	mW

Stereo Continuous Calibration DAC (CC-DAC)

TDA1311A

BLOCK DIAGRAM

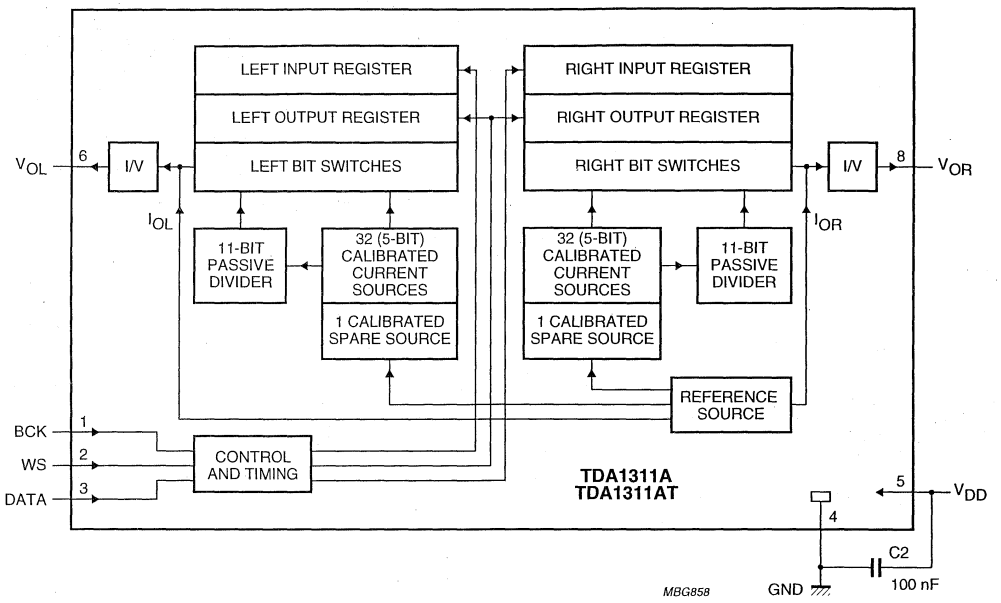


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage
V_{OL}	6	left channel output
n.c.	7	not connected
V_{OR}	8	right channel output

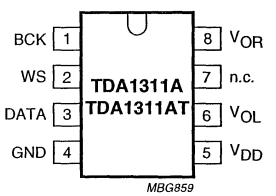


Fig.2 Pin configuration.

Quadruple filter DAC TDA1314T

FEATURES

- High dynamic range to enable digital DSP (Digital Signal Processor) volume control
- 18 bits data input format for each of the four channels
- Four times bit-serial oversampling filter
- 1st-order $4f_{as}$ (audio sampling frequency) noise shaper
- Four very low noise DACs
- Only 1st-order analog post filtering required
- Smooth power-on of the DAC output currents
- Because of the automatic digital PLL divider range setting the master clock is selectable in a wide $4f_{as}$ integer range
- Insensitive to jitter on the I^2S-bus signals with respect to the DAC total harmonic distortion deterioration.

APPLICATIONS

- Stand-alone quadruple low noise DAC
- Car radio DAC in conjunction with DSP.

GENERAL DESCRIPTION

The TDA1314T is a quadruple very low noise high dynamic range DAC which is intended for use in motor cars and is controlled by the car radio DSP. Each channel incorporates an 8th-order IIR up-sampling filter from 1ASF to 4ASF followed by a 1st-order noise shaper and DAC. The DAC currents are converted to audio voltage signals using operational amplifiers (one per channel).

QUICK REFERENCE DATA

V_{ref} = 2.5 and 5 V; T_{amb} = 25 °C; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$I_{O(DAC)}$	DAC output current (FS)	R_{ref} = 20.5 kΩ	±0.4	±0.5	±0.6	mA
$V_{O(DAC)}$	DAC output voltage, nominal DAC operational amplifier output voltage	$R_L \geq 5$ kΩ; R_{fb} = 3 kΩ	1.0	–	4.0	V
RES	DAC resolution	length of data input word	–	–	18	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; 0 dB signal level	–	–66	–56	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB signal level	92	96	–	dB
DS	digital silence	no signal; A-weighted	–	–110	–100	dB
P_{tot}	total power dissipation		–	85	–	mW
T_{amb}	operating ambient temperature		–40	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1314T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

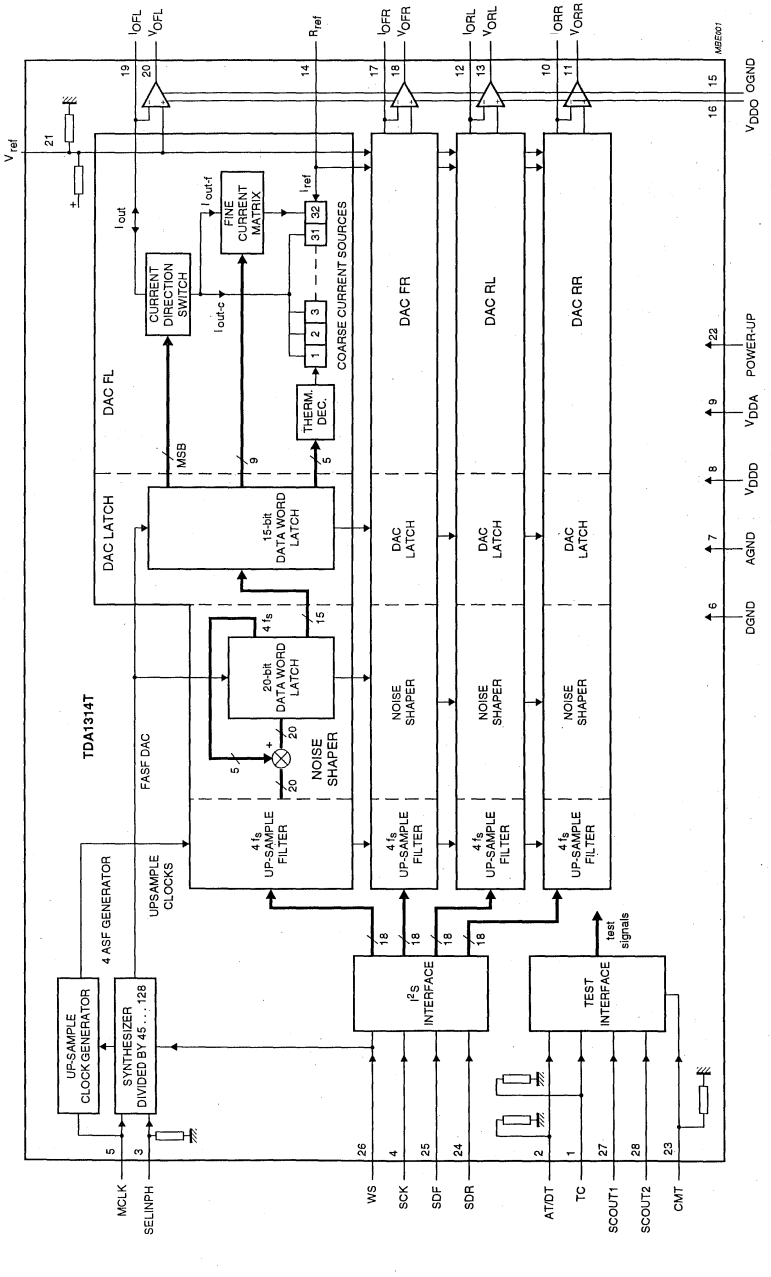


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TC	1	test control signal input (test/operational)
AT/DT	2	analog test/digital test select input
SELINPH	3	select in-phase $4f_{as}$ mode/scan input signal 1 in test mode
SCK	4	serial clock input; I^2S-bus
MCLK	5	master clock input; $f_i = N \times 4f_{as}$ ($45 \leq N \leq 128$)
DGND	6	digital ground
AGND	7	analog ground
V_{DDD}	8	digital supply voltage
V_{DDA}	9	analog supply voltage
I_{ORR}	10	DAC output current; rear right
V_{ORR}	11	DAC output voltage; rear right
I_{ORL}	12	DAC output current; rear left
V_{ORL}	13	DAC output voltage; rear left
R_{ref}	14	resistor reference input for DACs current
OGND	15	operational amplifier ground
V_{DDO}	16	operational amplifier supply
I_{OFR}	17	DAC output current; front right
V_{OFR}	18	DAC output voltage; front right
I_{OFL}	19	DAC output current; front left
V_{OFL}	20	DAC output voltage; front left
V_{ref}	21	reference voltage input ($\frac{1}{2}$ operational amplifier supply voltage)
POWER-UP	22	analog mute input for all DACs
CMT	23	current mirror input test signal
SDR	24	serial data input for rear DACs (I^2S-bus); scan input signal 2 in test mode
SDF	25	serial data input for front DACs (I^2S-bus)
WS	26	word select input (I^2S-bus)
SCOUT1	27	scan output signal 1 in test mode; $4f_{as}$ signal
SCOUT2	28	scan output signal 2 in test mode; PLL lock indicator

Digital audio input/output circuit (DAIO) TDA1315H

FEATURES

- Transceiver for SPDIF and *"IEC 958"* encoded signals
- High sensitivity input for transformer-coupled links
- TTL-level input for optical links
- Built-in IEC input selector
- Built-in IEC feed-through function
- Automatic sample frequency (f_s) detection
- System clock recovery from IEC input signal
- Low system clock drift when IEC input signal is removed
- Error detection and concealment
- PLL lock detection in transmit mode
- Serial audio interface conforms to I^2S-bus format
- Auxiliary I^2S-bus input for Analog-to-Digital Converter (ADC)
- Audio output selector
- Microcontroller-controlled and stand-alone mode
- 128-byte buffer for user data
- Bytewise exchange of user data with microcontroller
- Decoding of Compact Disc (CD) subcode Q-channel data
- Support for serial copy management system (SCMS)
- Light Emitting Diode (LED) drive capability (sample frequency and error indication)
- Pin-selectable device address for microcontroller interface
- Power-down mode.

GENERAL DESCRIPTION

The Digital Audio Input/Output circuit (DAIO) of the TDA1315H is a complete transceiver for biphase-mark encoded digital audio signals that conform to the SPDIF and *"IEC 958"* interface standards (consumer mode), made in the full CMOS-process C200.

In the receive mode, the device adjusts automatically to one of the three standardized sample frequencies (32, 44.1 or 48 kHz), decodes the input signal and separates audio and control data. A clock signal of either 256 or 384 times the sample frequency is generated to serve as a master clock signal in digital audio systems.

In the transmit mode, the device multiplexes the audio control and user data and encodes it for subsequent transmission via a cable or optical link.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	PIN POSITION	VERSION
TDA1315H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

All inputs are TTL compatible; all outputs are CMOS compatible; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{DDD} = V_{DDA}$	3.4	5.0	5.5	V
I_{DDAq}	analog quiescent current	PD = 1; T_{amb} = 25 °C	–	–	10	µA
I_{DDDq}	digital quiescent current	PD = 1; T_{amb} = 25 °C	–	–	10	µA
I_{DDA}	analog supply current	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	2.6	–	mA
I_{DDD}	digital supply current	f_s = 48 kHz; CLKSEL = 0	–	13	–	mA
Power						
P_{tot}	total power dissipation	f_s = 48 kHz; CLKSEL = 0; when IECIN1 input is used	–	80	–	mW
Temperature						
T_{amb}	operating ambient temperature		–20	–	+70	°C
IEC interface; pin IECIN1 (high sensitivity IEC input)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
Control part						
CHMODE, UNLOCK, $\overline{FS32}$, $\overline{FS44}$, $\overline{FS48}$ AND COPY (OPEN-DRAIN OUTPUTS)						
V_{OL}	LOW level output voltage	I_{OL} = 3 mA	–	–	0.5	V
RESET, SCK, LCLK, LMODE AND SYSCLKI (HYSTERESIS INPUTS)						
V_{tHL}	negative-going threshold	V_{DD} = 4.5 to 5.5 V	0.6	–	–	V
V_{tLH}	positive-going threshold	V_{DD} = 4.5 to 5.5 V	–	–	2.4	V
V_{hys}	input voltage hysteresis	V_{DD} = 4.5 to 5.5 V	–	0.7	–	V
Clock and timing						
V_{ref}	output reference voltage		–	2.1	–	V
RC_{int} (PIN 44)						
I_{CHfr}	charge-pump output current	frequency detector loop	–	±12	–	µA
I_{CHph}	charge-pump output current	phase detector loop	–	±24	–	µA

BLOCK DIAGRAM

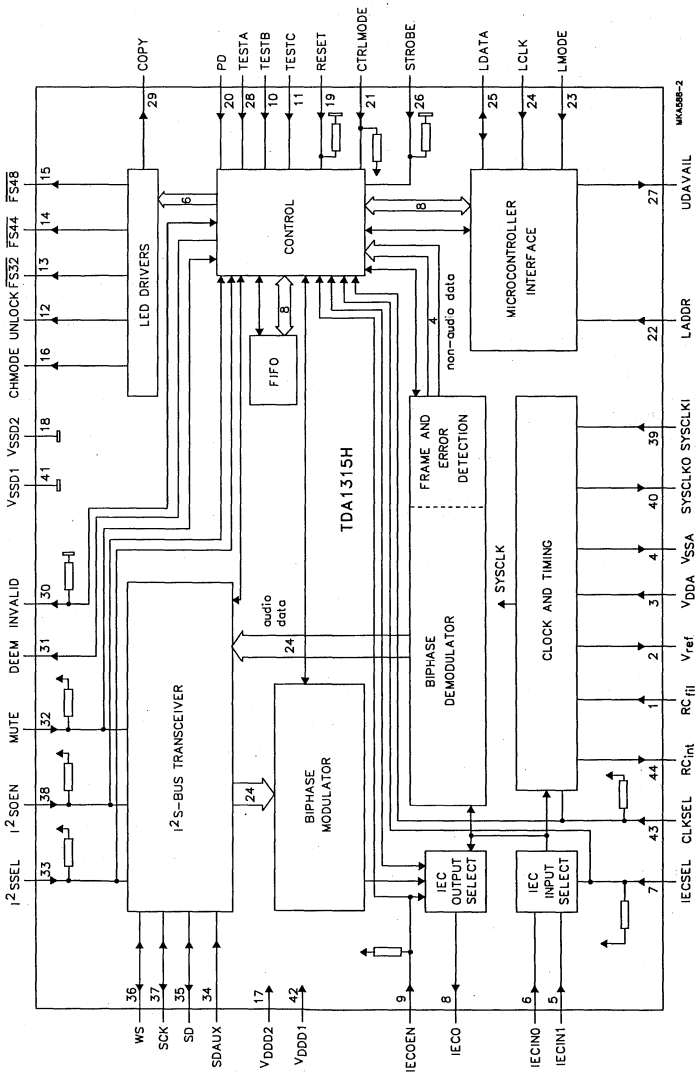


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	PADCELL	DESCRIPTION
RC_{fil}	1	E029	PLL loop filter input
V_{ref}	2	E029	decoupling internal reference voltage output
V_{DDA}	3	E008	analog supply voltage
V_{SSA}	4	E004	analog ground
IECIN1	5	E007	high sensitivity IEC input
IECIN0	6	IPP04	TTL level IEC input
IECSEL	7	IUP04	select IEC input 0 or 1 (0 = IECIN0; 1 = IECIN1); this input has an internal pull-up resistor
IECO	8	OPFH3	digital audio output for optical and transformer link
IECOEN	9	IUP04	digital audio output enable (0 = enabled; 1 = disabled/3-state); this input has an internal pull-up resistor
TESTB	10	IPP04	enable factory test input (0 = normal application; 1 = scan mode)
TESTC	11	IPP04	enable factory test input (0 = normal application; 1 = observation outputs)
UNLOCK	12	OPP41A	PLL out-of-lock (0 = not locked; 1 = locked); this output can drive an LED
$\overline{FS32}$	13	OPP41A	indicates sample frequency = 32 kHz (active LOW); this output can drive an LED
$\overline{FS44}$	14	OPP41A	indicates sample frequency = 44.1 kHz (active LOW); this output can drive an LED
$\overline{FS48}$	15	OPP41A	indicates sample frequency = 48 kHz (active LOW); this output can drive an LED
CHMODE	16	OPP41A	use of channel status block (0 = professional use; 1 = consumer use); this output can drive an LED
V_{DDD2}	17	E008	digital supply voltage 2
V_{SSD2}	18	E009	digital ground 2
RESET	19	IDP09	initialization after power-on, requires only an external capacitor connected to V_{DDD}; this is a Schmitt-trigger input with an internal pull-down resistor
PD	20	IPP04	enable power-down input in the standby mode (0 = normal application; 1 = standby mode)
CTRLMODE	21	IUP04	select microcontroller/stand-alone mode (0 = microcontroller; 1 = stand-alone); this input has an internal pull-up resistor
LADDR	22	IPP04	microcontroller interface address switch input (0 = 000001; 1 = 000010)
LMODE	23	IPP09	microcontroller interface mode line input
LCLK	24	IPP09	microcontroller interface clock line input
LDATA	25	IOF24	microcontroller interface data line input/output
STROBE	26	IDP04	strobe for control register (active HIGH); this input has an internal pull-down resistor
UDAVAIL	27	OPF23	synchronization for output user data (0 = data available; 1 = no data)
TESTA	28	IPP04	enable factory (scan) test input (0 = normal application; 1 = test clock enable)
COPY	29	OPP41A	copyright status bit (0 = copyright asserted; 1 = no copyright asserted); this output can drive an LED
INVALID	30	IOD24	validity of audio sample input/output (0 = valid sample; 1 = invalid sample); this pin has an internal pull-down resistor
DEEM	31	OPF23	pre-emphasis output bit (0 = no pre-emphasis; 1 = pre-emphasis)
MUTE	32	IUP04	audio mute input (0 = permanent mute; 1 = mute on receive error); this pin has an internal pull-up resistor

SYMBOL	PIN	PADCELL	DESCRIPTION
I^2SSEL	33	IUP04	select auxiliary input or normal input in transmit mode
SDAUX	34	IPP04	auxiliary serial data input; I^2S-bus
SD	35	IOF24	serial audio data input/output; I^2S-bus
WS	36	IOF24	word select input/output; I^2S-bus
SCK	37	IOF29	serial audio clock input/output; I^2S-bus
I^2SOEN	38	IUP04	serial audio output enable (0 = enabled; 1 = disabled/3-state); this input has an internal pull-up resistor
SYSCLKI	39	IPP09	system clock input (transmit mode)
SYSCLKO	40	OPFA3	system clock output (receive mode)
V_{SSD1}	41	E009	digital ground 1
V_{DDD1}	42	E008	digital supply voltage 1
CLKSEL	43	IUP04	select system clock (0 = $384f_s$; 1 = $256f_s$); this input has an internal pull-up resistor
RC_{int}	44	E029	integrating capacitor output

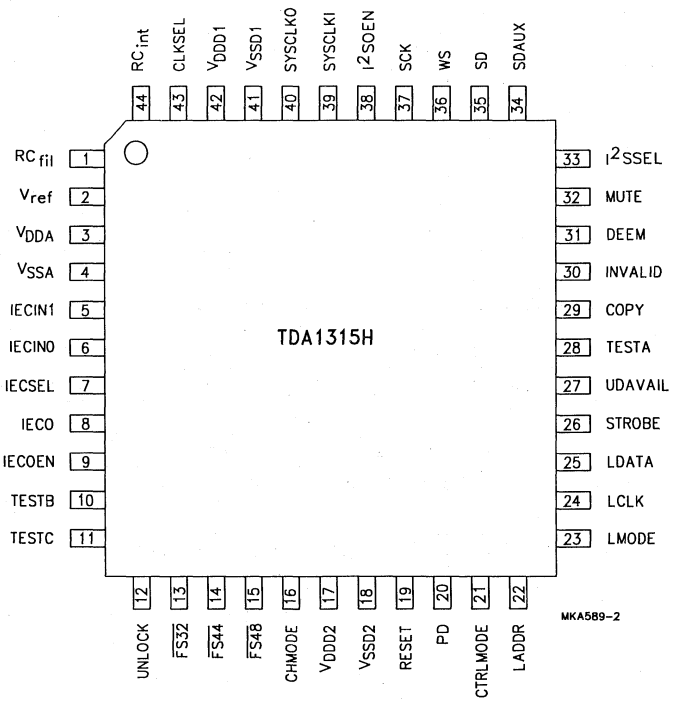


Fig.2 Pin configuration.

DCC read amplifier TDA1318

FEATURES

- Differential inputs for a low-power head configuration
- Low-noise current sources for the sense currents of the DCC head
- Reduced power consumption by separate on/off switching of the circuits and sense current of the DCC and CC parts of the IC
- The IC can be used with both the first and second generation DCC digital signal processing ICs
- High-impedance outputs in the OFF state so that the outputs of the ICs can be connected in parallel for dual decks or for decks with electrical auto-reverse heads
- AGC of DCC preamplifiers (can be switched off)
- Possibility of analog audio via DCC preamplifiers (analog via digital readers, ADR mode)
- Single 5 V supply.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1318 amplifies, filters and multiplexes signals arriving from magneto-resistive thin film heads (MRHs) which are suitable for DCC (Digital Compact Cassette) and CC (Compact Cassette) systems. The device also has current sources to provide sense currents through the DCC-MRHs and two amplifiers for magnetic feedback and biasing.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS[1]			MIN.	TYP.	MAX.	UNIT
		CS	SD	ADR				
V_{DD}	supply voltage	–	–	–	4.5	5.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers	–	–	–	4.5	5.0	5.5	V
I_{DDDCC}	supply current DCC mode (note 2)	1	1	0	–	31	41	mA
$I_{DDDCCadr}$	supply current DCC mode (ADR)	1	1	1	–	31	41	mA
I_{DDCC}	supply current CC mode	1	0	0	–	9.7	13	mA
$I_{DDCCadr}$	supply current CC mode (ADR)	1	0	1	–	17.8	24.5	mA
I_{CCM}	supply current feedback amplifiers	1	1	1	–	8.5	12	mA
		1	0	0				
		1	0	1				
I_{DD}	supply current (ADC reference ON)	0	1	–	–	1.6	2.2	mA
$I_{DD(Q)}$	total quiescent current in OFF mode	0	0	–	–	–	300	µA
P_{tot}	total power dissipation, DCC mode	–	–	–	–	250	–	mW
T_{amb}	operating ambient temperature	–	–	–	–30	–	+85	°C

Notes

1. In the conditions column 0 = LOW; 1 = HIGH.
2. ADR = 1 when pin INL and/or INR is connected to V_{SS}.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1318H	44	QFP44S10(1)	plastic	SOT307-2

Note

1. When using IR reflow soldering it is recommended that the Dry Packing instructions in the *"Quality Reference Pocket book"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

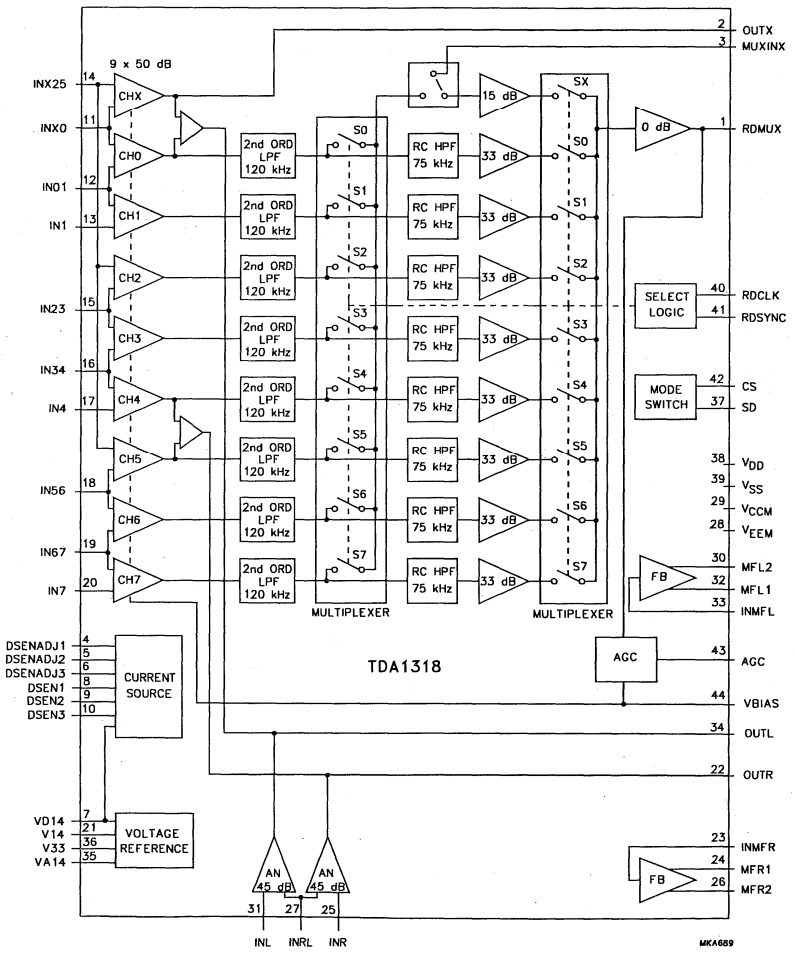


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RDMUX	1	output for sampled and multiplexed auxiliary and main data signals
OUTX	2	auxiliary channel preamplifier output
MUXINX	3	auxiliary channel multiplexer input
DSENAD J1	4	adjustment pin for DCC sense current 1
DSENAD J2	5	adjustment pin for DCC sense current 2
DSENAD J3	6	adjustment pin for DCC sense current 3
VD14	7	reference voltage output DCC sense
DSEN1	8	DCC sense current output 1
DSEN2	9	DCC sense current output 2
DSEN3	10	DCC sense current output 3
INX0	11	auxiliary channel input/channel 0 input
IN01	12	channels 0 and 1 input
IN1	13	channel 1 input
INX25	14	channels AUX, 2 and 5 input
IN23	15	channels 2 and 3 input
IN34	16	channels 3 and 4 input
IN4	17	channel 4 input
IN56	18	channels 5 and 6 input
IN67	19	channels 6 and 7 input
IN7	20	channel 7 input
V14	21	reference voltage output for DCC/analog inputs
OUTR	22	right channel analog output

SYMBOL	PIN	DESCRIPTION
INMFR	23	right channel feedback amplifier input
MFR1	24	right channel feedback amplifier output 1
INR	25	right channel analog input
MFR2	26	right channel feedback amplifier output 2
INRL	27	right/left channel analog input
V_{EEM}	28	ground for feedback amplifiers
V_{CCM}	29	positive supply for feedback amplifiers
MFL2	30	left channel feedback amplifier output 2
INL	31	left channel analog input
MFL1	32	left channel feedback amplifier output 1
INMFL	33	left channel feedback amplifier input
OUTL	34	left channel analog output
VA14	35	reference voltage output CC sense
V33	36	ADC reference voltage output
SD	37	select DCC part input
V_{DD}	38	positive supply voltage
V_{SS}	39	ground
RDCLK	40	read clock input
RDSYNC	41	read sync pulse input
CS	42	chip select input
AGC	43	AGC time constant
VBIAS	44	DCC preamplifier control voltage

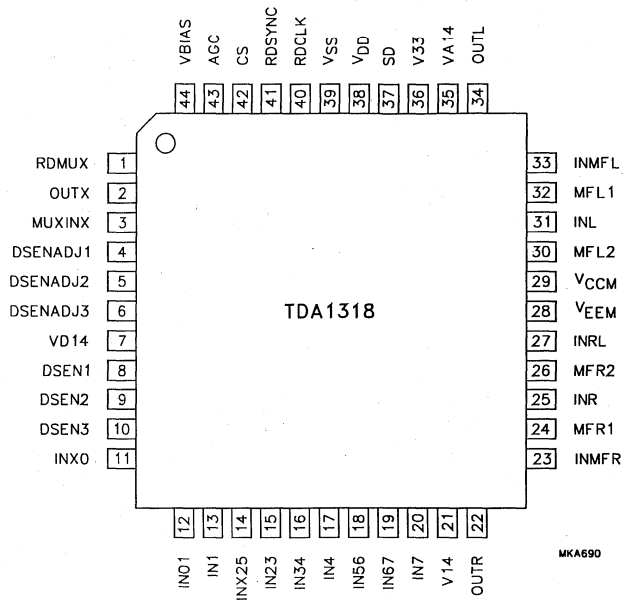


Fig.2 Pin configuration.

DCC write amplifier (write 2) TDA1319T

FEATURES

- Bidirectional high current output drivers
- Single point current setting
- Extra erase current for the auxiliary channel
- Increased current for auxiliary data
- Low standby power consumption
- Short-circuit protection to ground
- Serial data input
- Reduced RF emission due to slope control of write current.

GENERAL DESCRIPTION

The TDA1319T has been designed to drive an inductive recording head which is suitable for DCC (Digital Compact Cassette) systems.
The bidirectional current outputs are controlled by a two-wire serial bus. The amplitude of the write current can be set using an external resistor. The circuit can be switched to the standby mode to minimize supply current consumption.

DIGITAL dcc COMPACT CASSETTE

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.5	V
V_{DDO}	supply voltage (write outputs)		4.75	5.0	5.5	V
I_{DD}	supply current	note 1	–	7.5	11	mA
I_{DDO}	supply current (write outputs)	note 2	–	–	255	mA
		note 3	–	–	365	mA
		note 4	–	–	285	mA
I_{sb}	total standby current	note 5	–	2	3	mA
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. 1 kΩ erase adjust resistor connected between pins 5 and 6, no load at pin 9.
2. Momentary maximum value during write data; see Table 1; I_O = 225 mA.
3. Momentary maximum value during erase AUX; see Table 1 and Fig.5; resistor R_e connected between pins 5 and 6 (see Fig.7).
4. Momentary maximum value during write AUX; see Table 1; I_O = 255 mA.
5. Standby mode; see Table 1; $I_{sb} = I_{DD} + I_{DDO} + I_{clamp}$.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1319T	24	SO24L	plastic	SOT137-1

BLOCK DIAGRAM

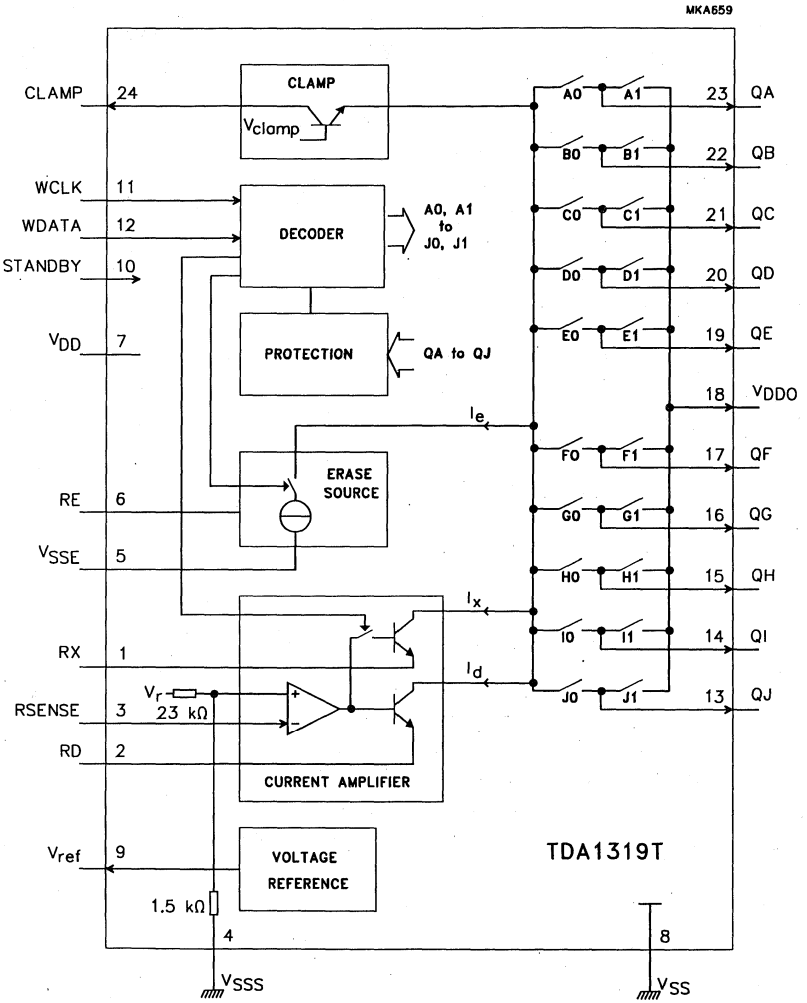


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RX	1	auxiliary current adjust resistor
RD	2	data current adjust resistor
RSENSE	3	sense voltage positive input
V_{SSS}	4	sense voltage ground
V_{SSE}	5	erase current source ground
RE	6	erase current adjust resistor
V_{DD}	7	supply voltage
V_{SS}	8	ground
V_{ref}	9	reference voltage output
STANDBY	10	standby mode control input
WCLK	11	write clock input
WDATA	12	write data input
QJ	13	write pulse output
QI	14	write pulse output
QH	15	write pulse output
QG	16	write pulse output
QF	17	write pulse output
V_{DDO}	18	supply voltage (write outputs)
QE	19	write pulse output
QD	20	write pulse output
QC	21	write pulse output
QB	22	write pulse output
QA	23	write pulse output
CLAMP	24	clamp current output

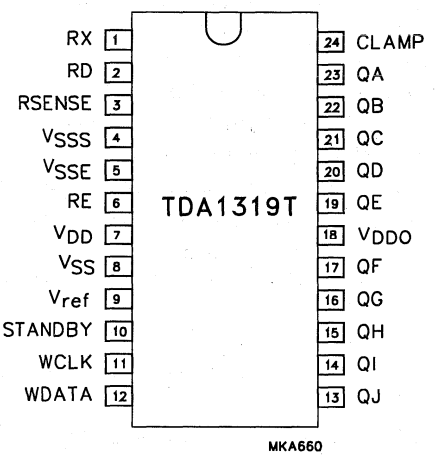
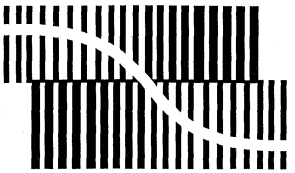


Fig.2 Pin configuration.

General Digital Input (GDIN) TDA1373H

FEATURES

- Four operating modes:
  - Sample Rate Conversion (SRC) mode
  - AD/DA mode
  - SLAVE-VCO mode
  - SLAVE-VCXO mode
- Full digital sample rate conversion over a wide range of input sample rates
- Fast and automatic detection and locking to the input sample rate with continuous tracking
- Digital Phase-Locked Loop (PLL) with adaptive bandwidth which removes jitter on the digital audio input
- Audio outputs (soft) muted during loop acquisition
- Full linear phase processing based on all-FIR filtering
- Integrated full digital IEC 958 demodulator for digital input signals (AES/EBU or SPDIF format) with intelligent error handling
- Extended input sample frequency range
- IEC 958 Channel Status (CS) and User Channel (UC) outputs
- On-chip CS and/or UC demodulation and buffering (consumer and professional format)
- Dedicated subcode processing for Compact Disc (CD)
- Final output quantization to 16, 18 or 20 bits with optional in-audio-band noise shaping
- Bitstream input and output for coupling with 1-bit analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC)
- I^2S and Japanese serial input formats supported for SRC and DAC functions
- I^2S and Japanese serial output formats supported for SRC and ADC functions
- I^2S and Japanese 4× oversampled serial output available for SRC and ADC functions
- 8-bit digital gain/attenuation control
- Switchable Digital Signal Processor (DSP)-interface (I^2S input and output) for additional audio processing
- Additional clock outputs available at 768, 384, 256 and $128f_{so}$
- 3-line serial microcontroller interface, compatible with the Philips CD I.C. protocol (HCL)



BITSTREAM CONVERSION

- 5 V power supply
- 0.7 µm double metal Complementary Metal Oxide Semiconductor (CMOS)
- SRC THD + N:
  - −113 dB over the 0 to 20 kHz band (1 kHz, 20 bits input and output) (see Fig.3)
  - −95 dB over the 0 to 20 kHz band (1 kHz, 16 bits input and output)
- Pass band ripple smaller than ±0.004 dB for up-sampling and down-sampling filters
- Stop band suppression:
  - selectable between 70 dB and 50 dB for 64× up-sampling filters
  - 80 dB for 128× down-sampling filters
- Microcontroller operated and stand-alone mode.

APPLICATIONS

- Professional audio equipment for:
  - mixing
  - recording
  - editing
  - broadcasting
- CD-Recordable (CD-R)
- Digital Speaker Systems (DSS)
- Digital Compact Cassette recorders (DCC)
- Digital Audio Tape (DAT) and MD recorders
- Digital amplifiers
- Jitter killers.

GENERAL DESCRIPTION

The TDA1373H is a General Digital Input (GDIN) device for audio signals which is able to perform a high-quality sample rate conversion of digital audio signals (**SRC mode**). The device reads several serial input formats and signals in the IEC 958 digital audio format (also known as AES/EBU or SPDIF signals). For this purpose a full Audio Digital Input Circuit (ADIC) is present in the device.

An internal digital PLL results in extensive jitter removal from incoming digital audio signals without any analog loop electronics. The standard 20 bit output word length can be limited to 16 or 18 bits by means of 'in-audio-band noise shaping'.

The GDIN digital filters can also be reused for Bitstream ADC and DAC conversion (**AD/DA mode**). The internal digital PLL can be reconfigured to operate the GDIN in a slave mode, where the output sample frequency of the device is locked to the incoming sample rate (**SLAVE-VCO** and **SLAVE-VCXO** modes).

The combination of an ADIC function, sample rate conversion and Bitstream ADC and DAC results in a device with a highly versatile functionality and large replacement value in consumer and professional audio sets.

QUICK REFERENCE DATA

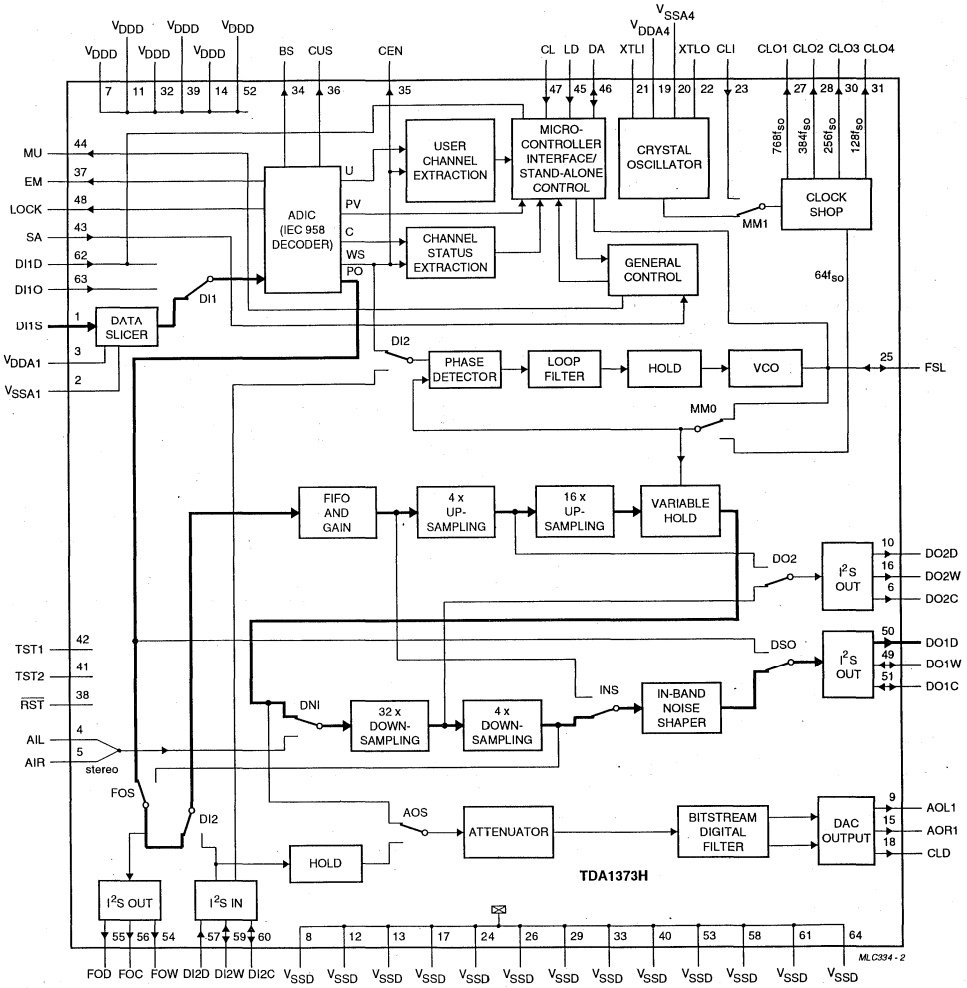
All inputs and outputs CMOS compatible; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	f_{so} > 44.1 kHz	4.75	5	5.5	V
		$f_{so} \leq$ 44.1 kHz	4.5	5	5.5	V
$I_{DD(tot)}$	total supply current	f_{so} = 44.1 kHz	–	155	–	mA
P_{tot}	total power dissipation	f_{so} = 44.1 kHz	–	775	–	mW
		f_{so} = 49 kHz; V_{DD} = 5.5 V	–	1030	–	mW
IEC 958 input DI1S (high-sensitivity IEC input)						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	–	V_{DD}	V
Clock and timing						
$f_{so(max)}$	maximum output sample frequency	V_{DD} = 4.75 V	49	55	–	kHz
Temperature						
T_{amb}	operating ambient temperature		0		70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1373H	QFP64	Plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.7 mm; high stand-off height	SOT319-1

BLOCK DIAGRAM



Switches MM1 and MM0 are controlled indirectly via the mode selection. All other switches can be controlled directly by the user.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
DI1S	1	IEC 958 digital audio input 'S' (200 mV peak-to-peak value)	E036A
V_{SSA1}	2	IEC 958 slicer analog ground	E038A
V_{DDA1}	3	IEC 958 slicer analog supply voltage	E037A
AIL	4	Bitstream audio input left	HPP01
AIR	5	Bitstream audio input right	HPP01
DO2C	6	serial digital audio output 2; bit clock output ($192f_{so}$)	OPF40
V_{DDD}	7	digital supply voltage; note 1	–
V_{SSD}	8	digital ground; note 2	–
AOL1	9	Bitstream audio output left	OPF40
DO2D	10	DLO = 0; serial digital audio output 2; data; DLO = 1; Bitstream audio output left inverted ($\overline{AOL1}$); note 3	OPF40
V_{DDD}	11	digital supply voltage; note 1	–
V_{SSD}	12	digital ground; note 2	–
V_{SSD}	13	digital ground; note 2	–
V_{DDD}	14	digital supply voltage; note 1	–
AOR1	15	Bitstream audio output right	OPF40
DO2W	16	DLO = 0; serial digital audio output 2; word select output ($4f_{so}$); DLO = 1; Bitstream audio output right inverted ($\overline{AOR1}$); note 3	OPF40
V_{SSD}	17	digital ground; note 2	–
CLD	18	Bitstream DAC clock (192 or $128f_{so}$)	OPF43
V_{DDA4}	19	oscillator analog supply voltage	E037A
V_{SSA4}	20	oscillator analog ground	E038A
XTLI	21	crystal input $768f_{so}$	OSX01
XTLO	22	crystal output	OSX01
CLI	23	external VCO input (SLAVE-VCO mode only)	HPP01
V_{SSD}	24	digital ground; note 2	–
FSL	25	SA = 0 (microcontroller operated) external VCO output (slave modes only); SA = 1 (stand-alone control) DI11 control line; note 4	HOF21
V_{SSD}	26	digital ground; note 2	–
CLO1	27	clock output $768f_{so}$	OPF40
CLO2	28	clock output $384f_{so}$	OPF40
V_{SSD}	29	digital ground; note 2	–
CLO3	30	clock output $256f_{so}$	OPF40
CLO4	31	clock output $128f_{so}$;	OPF40
V_{DDD}	32	digital supply voltage; note 1	–
V_{SSD}	33	digital ground; note 2	–
BS	34	block sync; channel status/user channel/CD subcode	OPF40
CEN	35	data enable; channel status/user channel/CD subcode	OPF40
CUS	36	data bit; channel status/user channel/CD subcode	OPF40
EM	37	IEC 958 source pre-emphasis flag	OPF20

SYMBOL	PIN	DESCRIPTION	TYPE
$\overline{RST}$	38	power-on reset input (active LOW)	HPP07
V_{DDD}	39	digital supply voltage; note 1	–
V_{SSD}	40	digital ground; note 2	–
TST2	41	test pin 2 (LOW for normal operation)	HPP01
TST1	42	test pin 1 (LOW for normal operation)	HPP01
SA	43	Stand-alone/microcontroller operated selection; SA = 1 for stand-alone operation	HPP01
MU	44	mute flag (active HIGH)	OPF40
LD	45	SA = 0 (microcontroller operated) microcontroller interface; load (read/write); SA = 1 (stand-alone control) NSD control line; note 4	HPP01
DA	46	SA = 0 (microcontroller operated) microcontroller interface (data); SA = 1 (stand-alone control) DI2 control line; note 4	HOF41
CL	47	SA = 0 (microcontroller operated) microcontroller interface (clock); SA = 1 (stand-alone control) QU1/QU0 control line; note 4	HPP01
LOCK	48	ADIC lock flag (active HIGH)	OPF40
DO1W	49	serial digital audio output 1; word select input/output (f_{so})	HOF41
DO1D	50	serial digital audio output 1; data	OPF43
DO1C	51	serial digital audio output 1; bit clock input/output ($48f_{so}$)	HOF41
V_{DDD}	52	digital supply voltage; note 1	–
V_{SSD}	53	digital ground; note 2	–
FOW	54	serial digital audio feature output; word select	OPF43
FOD	55	serial digital audio feature output; data	OPF43
FOC	56	serial digital audio feature output; bit clock ($64f_{so}$)	OPF43
DI2D	57	serial digital audio input 2; data	HPP01
V_{SSD}	58	digital ground; note 2	–
DI2W	59	serial digital audio input 2; word select	HOF21
DI2C	60	serial digital audio input 2; bit clock output	HOF21
V_{SSD}	61	digital ground; note 2	–
DI1D	62	SA = 0 (microcontroller operated) IEC 958 digital audio input 'D' (CMOS level); SA = 1 (stand-alone control) MSO control line; note 4	HPP01
DI1O	63	IEC 958 digital audio input 'O' (CMOS level)	HPP01
V_{SSD}	64	digital ground; note 2	–

Notes

1. All V_{DDD} pins are internally connected.
2. All V_{SSD} pins are internally connected.
3. DLO is a command flag from register 4 (see Section "Command registers").
4. SA is the stand-alone/microcontroller operated pin (pin 43). DI11, NSD, DI2, QU1, QU0 and MS0 are command flags to control the operation of the device. For more information see Section "Controlling the GDIN".

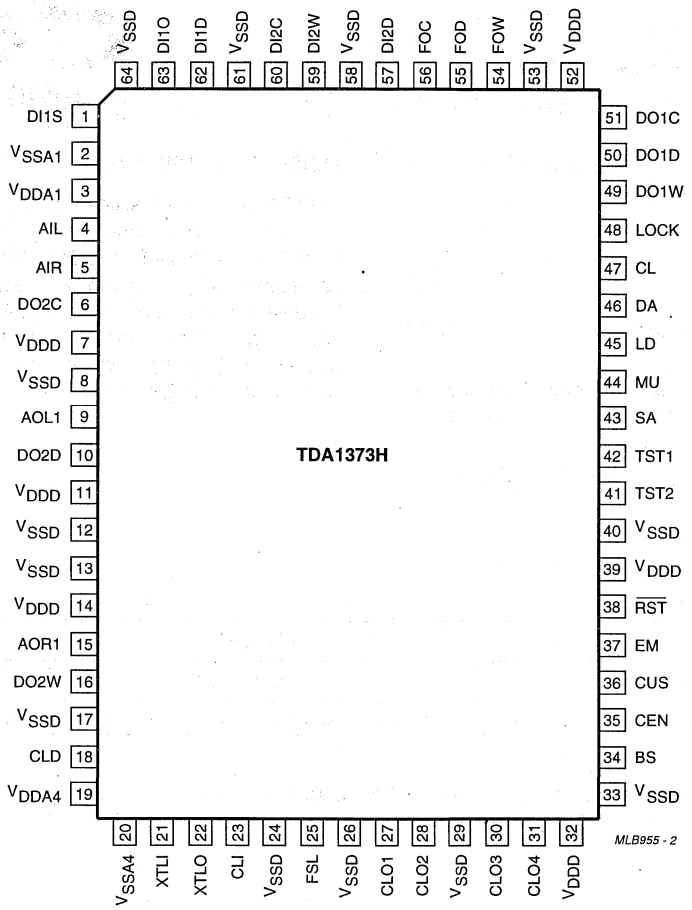


Fig.2 Pin configuration.

DCC read amplifier (READ 3) TDA1380

FEATURES

- Single 3 V supply
- Low power consumption
- Differential inputs for low power head configuration
- Can be used with 1st, 2nd and 3rd generation digital signal processing ICs
- Automatic gain control for DCC preamplifiers
- Selectable input amplifiers for A or B side of cassette
- ACC playback via DCC preamplifiers
- Uncommitted amplifiers for equalization during ACC playback
- Low noise current sources for the sense currents of the DCC heads
- Generates reference sense current for temperature compensation of the write current, in recordable application with the TDA1381
- High feedback application possible (for adjustment minimization)
- Suitable for digital post-processor.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1380 amplifies, filters and multiplexes signals that are input from an 18-channel magnetoresistive thin film head (MRH) suitable for the DCC (Digital Compact Cassette) and ACC (Analog Compact Cassette) systems. The device also contains current sources to provide sense currents through the heads and amplifiers for magnetic feedback and biasing. Two uncommitted amplifiers are available for analog equalization.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1380	TQFP64[1]	plastic thin quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"*; (order number 9398 510 63011) are followed.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS ON PINS[1]			MIN.	TYP.	MAX.	UNIT
		CS	SA	AB				
V_{DD}	supply voltage	–	–	–	2.7	3.0	5.5	V
V_{CCM}	supply voltage feedback amplifiers	–	–	–	2.7	3.0	5.5	V
$I_{DDDCC} + I_{CCM}$	supply current DCC mode	1	0	X	28	39	53	mA
$I_{DDACC} + I_{CCM}$	supply current ACC mode	1	1	X	26	35	47	mA
I_{DDRS}	supply current reference sense current mode	0	0	X	0.6	1.2	1.6	mA
I_{DDAB}	supply current sense AB mode	0	1	1	1.5	2.7	3.7	mA
$I_{DDstb} + I_{CCM}$	supply current standby mode	0	1	0	–	0.2	0.3	mA
$P_{(tot)DCC}$	total power dissipation DCC mode; note 2	1	0	X	–	120	–	mW
$P_{(tot)ACC}$	total power dissipation ACC mode; note 2	1	1	X	–	105	–	mW
T_{amb}	operating ambient temperature	–	–	–	−30	–	+85	°C

Notes

1. In the conditions column 0 = LOW; 1 = HIGH; X = don't care.
2. $V_{DD} = V_{CCM} = 3$ V; $I_{DSEN} = 0$; $I_{FB} = 0$.

BLOCK DIAGRAM

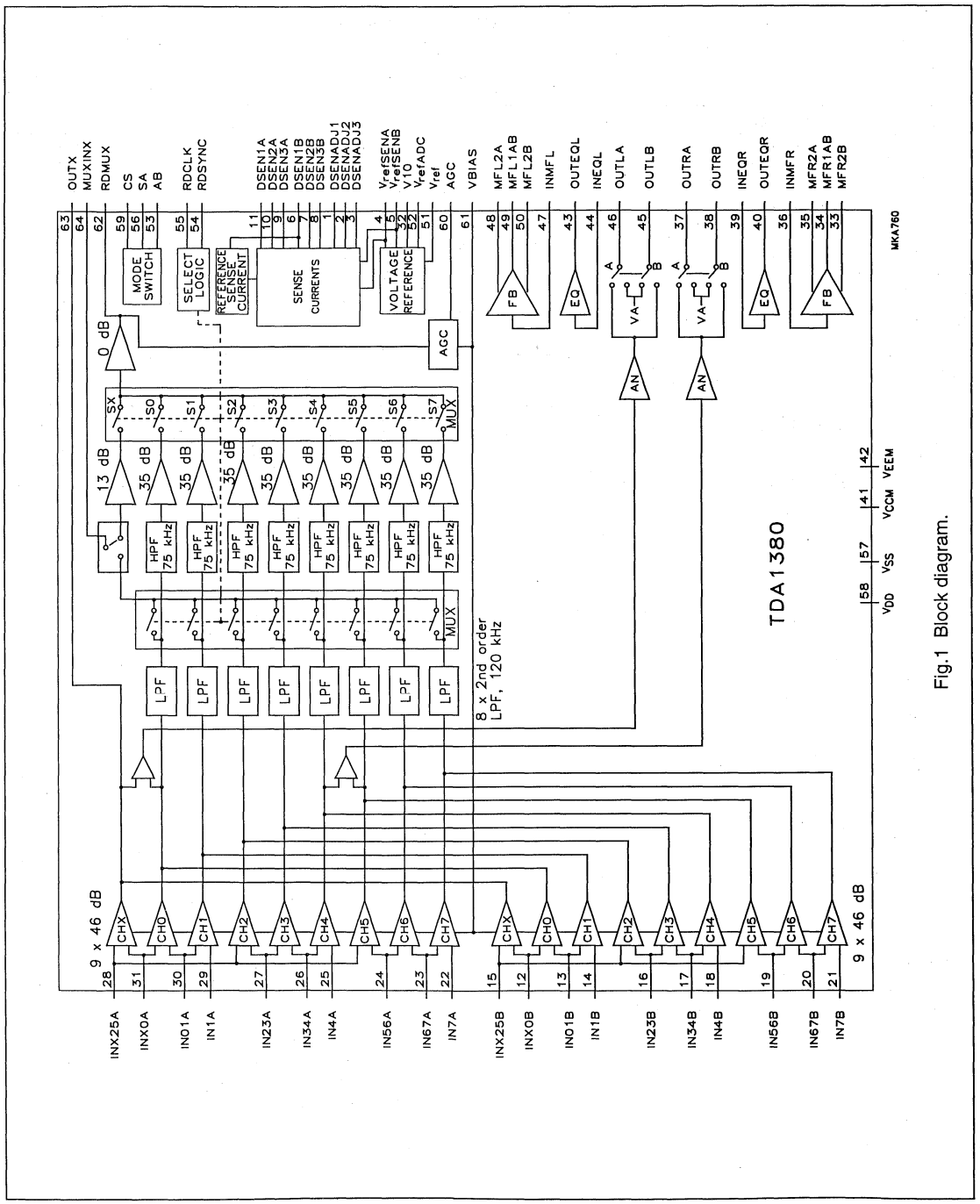


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DSENADJ1	1	adjustment pin for sense current 1 (A and B)
DSENADJ2	2	adjustment pin for sense current 2 (A and B)
DSENADJ3	3	adjustment pin for sense current 3 (A and B)
$V_{refSENA}$	4	reference voltage output sense (A)
$V_{refSENB}$	5	reference voltage output sense (B)
DSEN1B	6	sense current output 1 (B)
DSEN2B	7	sense current output 2 (B)
DSEN3B	8	sense current output 3 (B)
DSEN3A	9	sense current output 3 (A)
DSEN2A	10	sense current output 2 (A)
DSEN1A	11	sense current output 1 (A)
INX0B	12	auxiliary channel input/channel 0 input (B)
IN01B	13	channel 0 and 1 input (B)
IN1B	14	channel 1 input (B)
INX25B	15	channels AUX, 2 and 5 input (B)
IN23B	16	channels 2 and 3 input (B)
IN34B	17	channels 3 and 4 input (B)
IN4B	18	channel 4 input (B)
IN56B	19	channels 5 and 6 input (B)
IN67B	20	channels 6 and 7 input (B)
IN7B	21	channel 7 input (B)
IN7A	22	channel 7 input (A)
IN67A	23	channels 6 and 7 input (A)
IN56A	24	channels 5 and 6 input (A)
IN4A	25	channel 4 input (A)
IN34A	26	channels 3 and 4 input (A)
IN23A	27	channels 2 and 3 input (A)
INX25A	28	channels AUX, 2 and 5 input (A)
IN1A	29	channel 1 input (A)
IN01A	30	channels 0 and 1 input (A)
INX0A	31	auxiliary channel input/channel 0 input (A)
V10	32	reference voltage for DCC inputs
MFR2B	33	right channel feedback amplifier output 2 (B)
MFR1AB	34	right channel feedback amplifier output 1 (A and B)

SYMBOL	PIN	DESCRIPTION
MFR2A	35	right channel feedback amplifier output 2 (A)
INMFR	36	right channel feedback amplifier input
OUTRA	37	right channel ACC output (A)
OUTRB	38	right channel ACC output (B)
INEQR	39	right channel equalization amplifier input
OUTEQR	40	right channel equalization amplifier output
V_{CCM}	41	supply voltage for feedback amplifiers
V_{EEM}	42	ground for feedback amplifiers
OUTEQL	43	left channel equalization amplifier output
INEQL	44	left channel equalization amplifier input
OUTLB	45	left channel ACC output (B)
OUTLA	46	left channel ACC output (A)
INMFL	47	left channel feedback amplifier input
MFL2A	48	left channel feedback amplifier output 2 (A)
MFL1AB	49	left channel feedback amplifier output 1 (A and B)
MFL2B	50	left channel feedback amplifier output 2 (B)
V_{ref}	51	reference voltage output
V_{refADC}	52	ADC reference voltage output
AB	53	tape sector A or B selection input
RDSYNC	54	read sync pulse input
RDCLK	55	read clock pulse input
SA	56	select ACC mode input
V_{SS}	57	ground
V_{DD}	58	supply voltage
CS	59	chip select input
AGC	60	AGC time constant
VBIAS	61	preamplifier gain control voltage input
RDMUX	62	output of sampled and multiplexed auxiliary and main data signals
OUTX	63	auxiliary channel preamplifier output
MUXINX	64	auxiliary channel multiplexer input

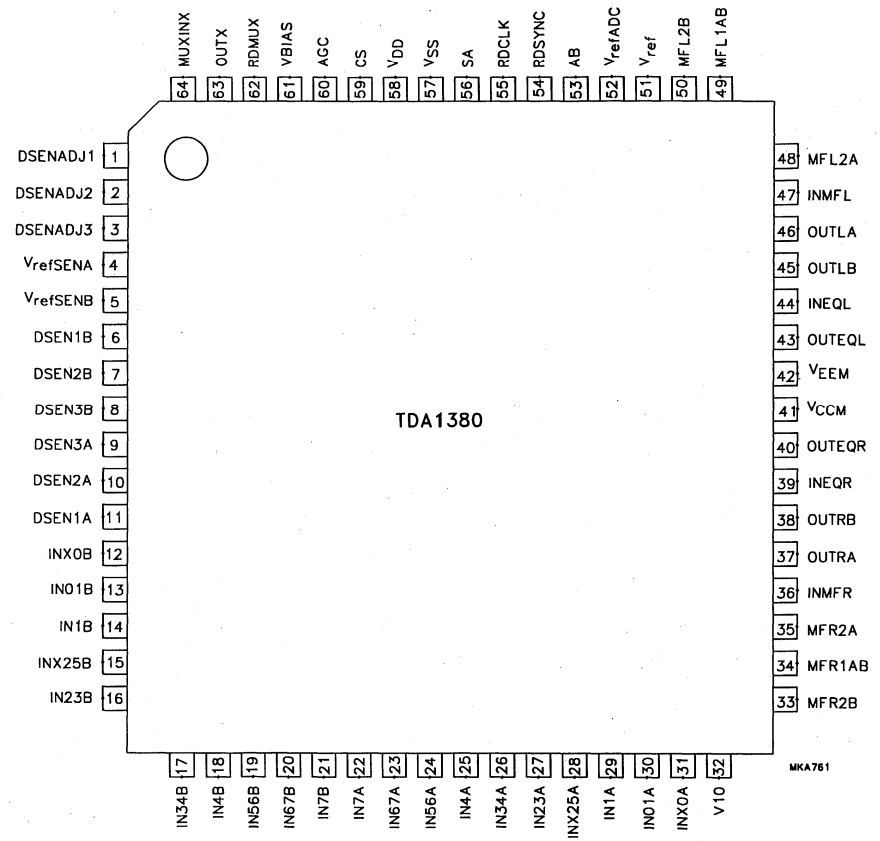


Fig.2 Pin configuration.

DCC write amplifier (WRITE3) TDA1381

FEATURES

- Single 3 V power supply
- Low standby current consumption
- 20 bidirectional current outputs (2 × nine heads)
- Single point main data and auxiliary current setting
- Reduction of power consumption between write pulses
- Soft switching of output currents
- Serial data input
- Timing is compatible with TDA1319T
- Uncommitted operational amplifier available.

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1381 has been designed to drive an 18-channel inductive recording head which is suitable for the DCC (Digital Compact Cassette) system. The bidirectional current outputs are controlled by a two-wire serial bus. The amplitude of the write current pulses can be set by either voltage or current control. The circuit can be switched to standby mode to minimize supply current consumption.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	3.0	4.0	V
I_{DD}	supply current	note 1	–	9	12	mA
$I_{DD(av)}$	average supply current	note 2	–	26.5	–	mA
I_{stb}	total standby current		–	0.1	0.3	mA
$I_{WDAT(max)}$	maximum write current for main data channels 0 to 7	note 3	100	–	–	mA
$I_{WAUX(max)}$	maximum write current for auxiliary channel	note 3	115	–	–	mA
$I_{EAUX(max)}$	maximum erase current for auxiliary channel	note 3	153	–	–	mA
$P_{d(av)}$	average power dissipation	note 2	–	80	–	mW
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. No head connected; all outputs unloaded; V_{DD} = 3 V.
2. In the auxiliary and data write mode; writing DCC data; I_{WDAT} = 60 mA; V_{DD} = 3 V; f_{clk} = 3.072 MHz. Data channels resistively loaded with 6 Ω, auxiliary channel resistively loaded with 4 Ω between pins 23 and 24, and 37 and 38.
3. Resistors connected in accordance with test circuit of Fig.7.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1381H	TQFP48(1)	plastic thin quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

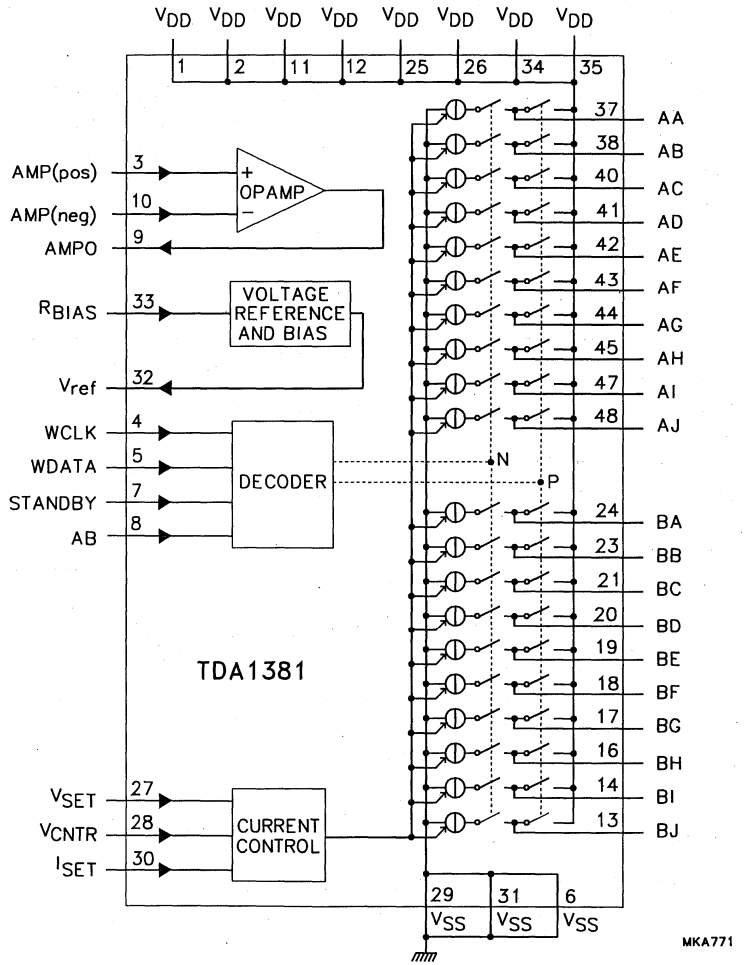


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DD}	1	supply voltage
V_{DD}	2	supply voltage
AMP(pos)	3	operational amplifier non-inverting input
WCLK	4	write clock input
WDATA	5	write data input
V_{SS}	6	ground
STANDBY	7	standby mode control input
AB	8	tape sector A or B select input
AMPO	9	operational amplifier output
AMP(neg)	10	operational amplifier inverting input
V_{DD}	11	supply voltage
V_{DD}	12	supply voltage
BJ	13	sector B write pulse output J
BI	14	sector B write pulse output I
n.c.	15	not connected
BH	16	sector B write pulse output H
BG	17	sector B write pulse output G
BF	18	sector B write pulse output F
BE	19	sector B write pulse output E
BD	20	sector B write pulse output D
BC	21	sector B write pulse output C
n.c.	22	not connected
BB	23	sector B write pulse output B
BA	24	sector B write pulse output A
V_{DD}	25	supply voltage
V_{DD}	26	supply voltage
V_{SET}	27	control voltage input
V_{CNTR}	28	voltage-to-current conversion setting input
V_{SS}	29	ground
I_{SET}	30	control current input
V_{SS}	31	ground
V_{ref}	32	reference voltage output
R_{BIAS}	33	bias current resistor
V_{DD}	34	supply voltage
V_{DD}	35	supply voltage
n.c.	36	not connected
AA	37	sector A write pulse output A
AB	38	sector A write pulse output B
n.c.	39	not connected
AC	40	sector A write pulse output C

SYMBOL	PIN	DESCRIPTION
AD	41	sector A write pulse output D
AE	42	sector A write pulse output E
AF	43	sector A write pulse output F
AG	44	sector A write pulse output G
AH	45	sector A write pulse output H
n.c.	46	not connected
AI	47	sector A write pulse output I
AJ	48	sector A write pulse output J

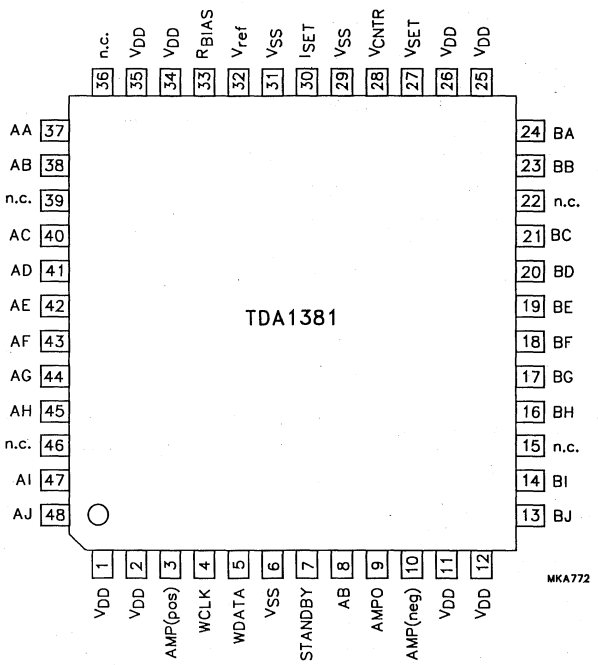


Fig.2 Pin configuration.

DCC record/playback amplifier TDA1383

FEATURES

General

- Single 3 V power supply
- Low standby current consumption
- Internal voltage regulator for improved supply ripple rejection
- Double-speed DCC record and playback
- Can be applied with all generations of digital processing ICs
- All gains and settings are software controlled
- Reduced number of external components.

Record part

- Single point main data and AUX data record current setting
- Reduction of power consumption between current pulses
- Accurate temperature compensation of the record current by measuring the tape temperature
- Soft switching of record currents
- Timing compatible with TDA1319T and TDA1381H.

Playback part

- Low noise amplifiers
- Pre-equalization and anti-aliasing filters
- Automatic gain control of DCC preamplifiers
- Optional recording of auxiliary data during DCC playback
- Auxiliary data detect after record e.g. to detect end of tape or 'head clogging'
- Two amplifiers for ACC equalization
- Control signal for ferro/chrome switches
- Mute for ACC playback
- Music search function during ACC (re)wind (to be confirmed).

DIGITAL dcc COMPACT CASSETTE

GENERAL DESCRIPTION

The TDA1383 is a single-chip record and playback amplifier for a Digital Compact Cassette (DCC) tapedeck, including Analog Compact Cassette (ACC) playback functions. The device is designed to be used with the Philips DCC head, type RP410R1/15. All modes of operation and settings can be controlled by a single serial input. Application of the TDA1383 provides a small, versatile, low power and inexpensive DCC front-end.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1383H	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

QUICK REFERENCE DATA

T_{amb} = 25 °C; $V_{DD1} = V_{DD2}$ = 3.3 V; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage 1 record part		2.7	3.3	5.5	V
V_{DD1}	supply voltage 1 record part and playback part	note 1	tbf	3.3	5.5	V
V_{DD2}	supply voltage 2 playback part		2.7	3.3	5.5	V
$I_{DD1} + I_{DD2}$	supply current	DCC record mode; I_D = 100 mA	–	45	60	mA
		DCC playback mode; I_{sense} = 3 mA	–	52	68	mA
		ACC playback mode; I_{sense} = 3 mA	–	29	38	mA
I_{stb}	total standby supply current	no clock; note 1	–	–	50	µA
I_D	record current main data channels 0 to 7	see Table 1	10	–	125	mA
I_{AUX}	record/erase current auxiliary data channel		10	–	153	mA
$P_{d(av)}$	average power dissipation	DCC record mode; I_D = 100 mA	–	130	–	mW
		DCC playback mode; I_{sense} = 3 mA	–	150	–	mW
		ACC playback mode; I_{sense} = 3 mA	–	85	–	mW
T_{amb}	operating ambient temperature		–30	–	+85	°C

Note

1. V_{DD2} is not connected to V_{DD1} (internal voltage regulator on).

Table 1 Maximum record current as a function of V_{DD1} and record head resistance

V_{DD1}	R_{rec} = 10 Ω	R_{rec} = 6.5 Ω	R_{rec} = 4 Ω
2.7 V	75	90	110
3.3 V	90	110	125
>4 V	125	125	125

BLOCK DIAGRAM

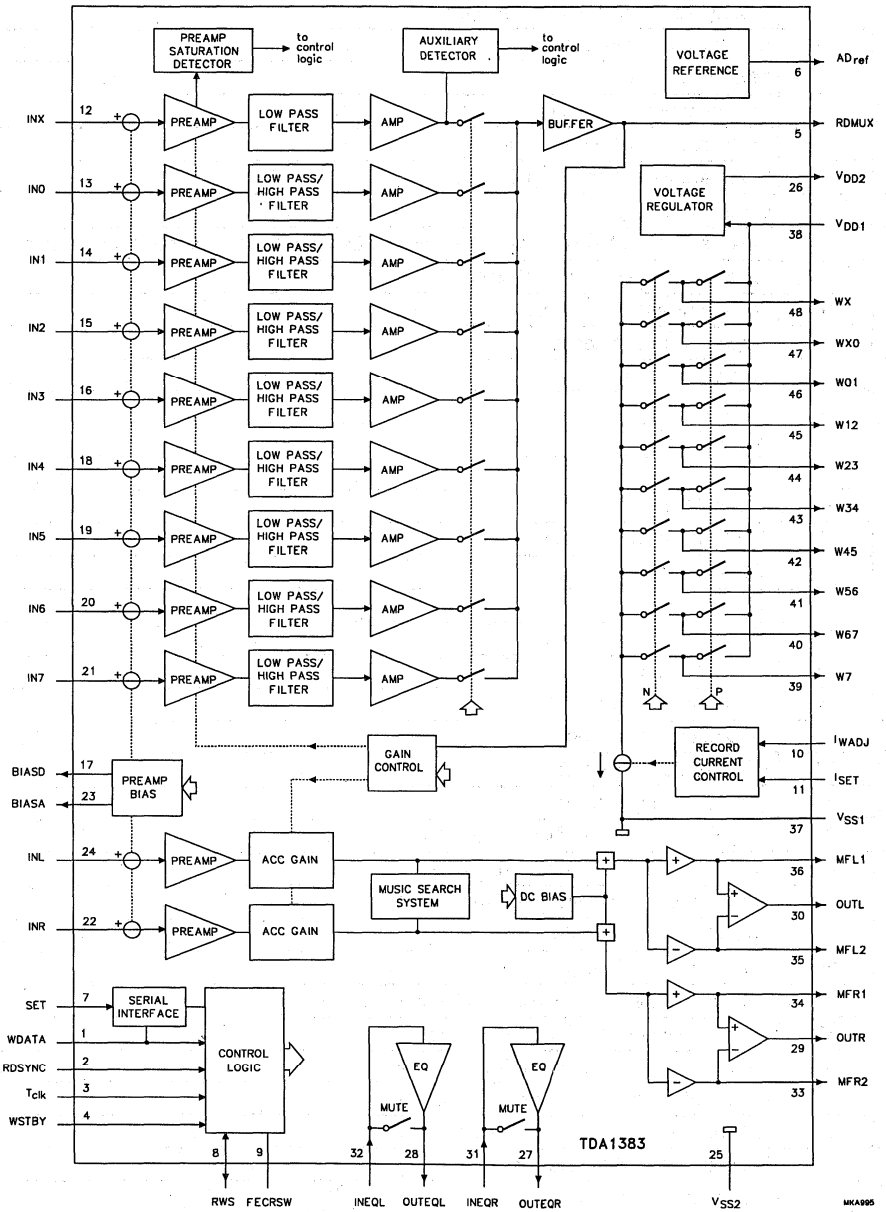


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
WDATA	1	record data input/control data input
RDSYNC	2	playback sync input
T_{CLK}	3	tape clock input
WSTBY	4	record standby control input
RDMUX	5	multiplexed DCC data output
AD_{ref}	6	AD reference voltage output
SET	7	control data input
RWS	8	music search output/AUX detector output/saturation detector output/external clock input
FECRSW	9	ferro-chrome switch control signal
I_{WADJ}	10	record current adjust input
I_{SET}	11	record current set input
INX	12	auxiliary channel input
IN0	13	channel 0 input
IN1	14	channel 1 input
IN2	15	channel 2 input
IN3	16	channel 3 input
BIASD	17	DCC bias voltage output
IN4	18	channel 4 input
IN5	19	channel 5 input
IN6	20	channel 6 input
IN7	21	channel 7 input
INR	22	ACC right channel input
BIASA	23	ACC bias voltage output
INL	24	ACC left channel input
V_{SS2}	25	ground for playback part
V_{DD2}	26	supply voltage for playback part/voltage regulator output
OUTEQR	27	right channel equalization amplifier output
OUTEQL	28	left channel equalization amplifier output
OUTR	29	right channel ACC output
OUTL	30	left channel ACC output
INEQR	31	right channel equalization amplifier input
INEQL	32	left channel equalization amplifier input
MFR2	33	right channel feedback amplifier output 2
MFR1	34	right channel feedback amplifier output 1
MFL2	35	left channel feedback amplifier output 2
MFL1	36	left channel feedback amplifier output 1
V_{SS1}	37	ground for record part (substrate)
V_{DD1}	38	supply voltage for record part
W7	39	channel 7 record current output
W67	40	channel 6/7 record current output

SYMBOL	PIN	DESCRIPTION
W56	41	channel 5/6 record current output
W45	42	channel 4/5 record current output
W34	43	channel 3/4 record current output
W23	44	channel 2/3 record current output
W12	45	channel 1/2 record current output
W01	46	channel 0/1 record current output
WX0	47	channel X/0 record current output
WX	48	channel X record current output

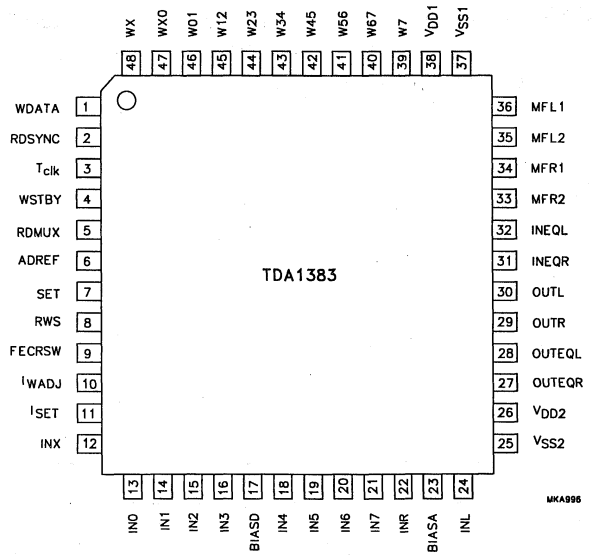


Fig.2 Pin configuration.

Noise shaping filter DAC TDA1386T

FEATURES

General

- Double-speed mode
- Digital volume control
- Soft mute function
- 12 dB attenuation
- Low power dissipation
- Digital de-emphasis.

Easy application

- Voltage output
- Only 1st-order analog post-filtering required
- Operational amplifiers and digital filter integrated
- $256f_s$ system clock (f_{sys})
- I^2S-bus or 16, 18 or 20 bits LSB fixed serial input format
- Single rail supply.

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- No zero crossing distortion
- Inherently monotonic
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

GENERAL DESCRIPTION

The TDA1386T is a dual CMOS digital-to-analog converter with up-sampling filter and noise shaper. The combination of oversampling up to $4f_s$, noise shaping and continuous calibration conversion ensures that only simple 1st order analog post filtering is required.

The TDA1386T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB fixed serial data input format with word lengths of 16, 18 or 20 bits. Two cascaded IIR filters increase the sampling rate 4 times.

The DACs are of the continuous calibration type and incorporate a special data coding. This ensures a high signal-to-noise ratio, wide dynamic range and immunity to process variation and component ageing.

Two on-board operational amplifiers convert the digital-to-analog current to an output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1386T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

QUICK REFERENCE DATA

All power supply pins V_{DD} and GND must be connected to the same external supply unit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current	V_{DDD} = 5 V; at code 00000H	–	5	8	mA
I_{DDA}	analog supply current	V_{DDA} = 5 V; at code 00000H	–	3	5	mA
I_{DDO}	operational amplifier supply current	V_{DDO} = 5 V; at code 00000H	–	2	4	mA
Analog signals						
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO}$ = 5 V; R_{OL} > 5 kΩ	0.935	1.1	1.265	V
R_L	output load resistance		5	–	–	kΩ
DAC performance						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; f_i = 1 kHz	–	–70	–	dB
			–	0.032	–	%
		at –60 dB signal level; f_i = 1 kHz	–	–42	–32	dB
			–	0.8	2.5	%
S/N_{ds}	signal-to-noise ratio at digital silence	no signal; A-weighted	–	–108	–96	dB
BR	input bit rate at data input	f_s = 44.1 kHz; normal speed	–	–	2.822	bits
		f_s = 44.1 kHz; double speed	–	–	5.645	bits
f_{sys}	clock frequency		6.4	–	18.432	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

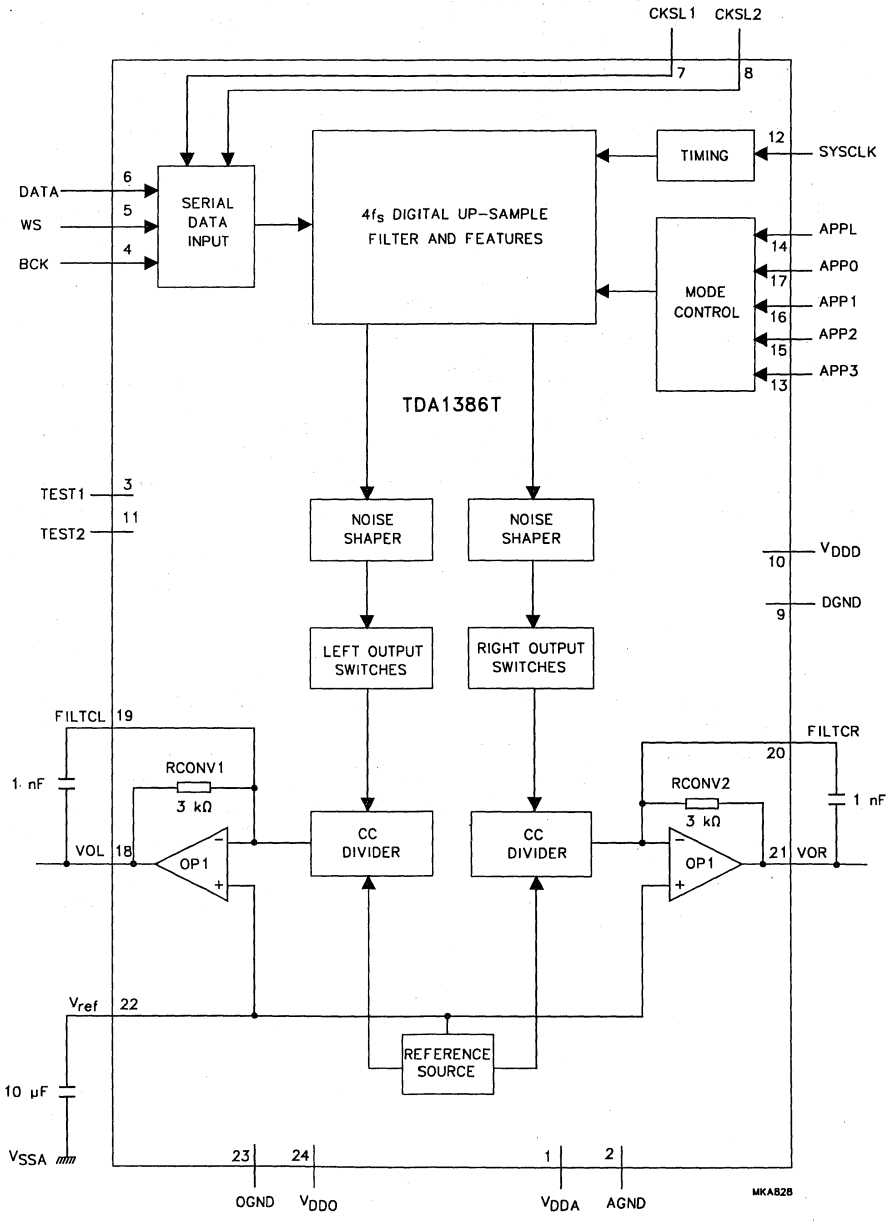


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	analog supply voltage
AGND	2	analog ground
TEST1	3	test input 1; pin should be connected to DGND
BCK	4	bit clock input
WS	5	word select input
DATA	6	data input
CKSL1	7	format selection 1
CKSL2	8	format selection 2
DGND	9	digital ground
V_{DDD}	10	digital supply voltage
TEST2	11	test input 2; pin should be connected to DGND
SYSCLK	12	system clock $256f_s$
APP3	13	application mode 3 input
APPL	14	application mode selection input
APP2	15	application mode 2 input
APP1	16	application mode 1 input
APP0	17	application mode 0 input
VOL	18	left channel output
FILTCL	19	capacitor for left channel 1st-order filter function, should be connected between pins 19 and 18
FILTCR	20	capacitor for right channel 1st-order filter function, should be connected between pins 20 and 21
VOR	21	right channel output
V_{ref}	22	internal reference voltage for output channels ($0.5V_{DDO}$ typ.)
OGND	23	operational amplifier ground
V_{DDO}	24	operational amplifier supply voltage

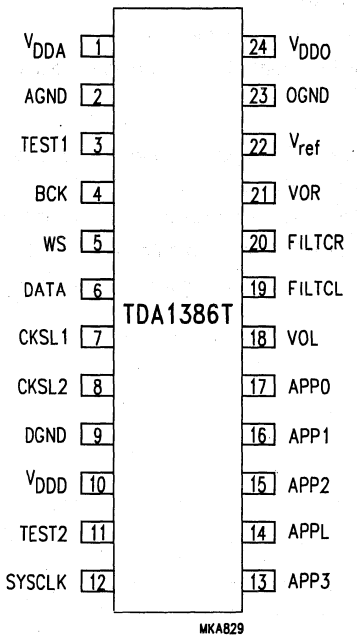


Fig.2 Pin configuration.

Stereo Continuous Calibration DAC (CC-DAC) TDA1387T

FEATURES

- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Single 3 to 5.5 V supply rail
- Output and bias current are proportional to the supply voltage
- Fast settling time enables 2, 4 and 8 times oversampling (serial input) or double-speed operation at 4 times oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (–40 to + 85 °C)
- I^2S-bus input format (time multiplex, two's complement, TTL)
- No zero-crossing distortion
- Large DC output voltage compliance
- Contained in small outline package.

APPLICATIONS

- Portable digital audio equipment.

GENERAL DESCRIPTION

The TDA1387T is a member of a generation of digital-to-analog converters which incorporates the innovative technique of Continuous Calibration. The largest bit currents are repeatedly generated from one single reference current. This duplication is based upon an internal charge storage principle and has an accuracy which is insensitive to ageing, temperature and process variations.

The TDA1387T is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. The intrinsic high coarse current accuracy combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensure high quality audio reproduction. The CC-DAC is eminently suitable for use in portable digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1387T	SO8	plastic small outline package; 8 leads; body width 3.9 mm.	SOT96-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V at code 0000H	–	5.5	6.5	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.86	1.0	1.14	mA
		V_{DD} = 3 V	–	0.6	–	mA
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–78	dB
		at 0 dB signal level	–	0.004	0.012	%
		at –60 dB signal level	–	–33	–24	dB
		at –60 dB signal level	–	2.2	6	%
		at –60 dB; A-weighted	–	–35	–	dB
		at –60 dB; A-weighted	–	1.7	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	98	–	dB
t_{cs}	current settling time to ±1 LSB		–	0.2	–	µs
BR	input bit rate (pin 3)		–	–	18.4	Mbits/s
f_{clk}	clock frequency		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at pins 6 and 8		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	°C
P_{tot}	total power dissipation	V_{DD} = 5 V at code 0000H	–	27.5	36	mW
		V_{DD} = 3 V at code 0000H	–	10	–	mW

BLOCK DIAGRAM

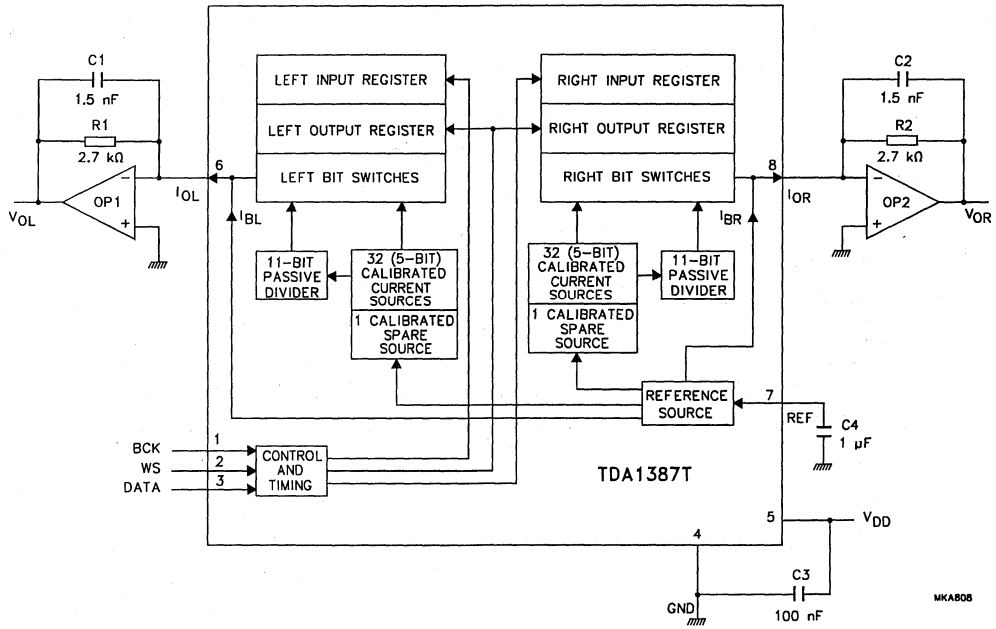


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word selection input
DATA	3	data input
GND	4	ground
V_{DD}	5	supply voltage input
I_{OL}	6	left channel output
REF	7	reference decoupling
I_{OR}	8	right channel output

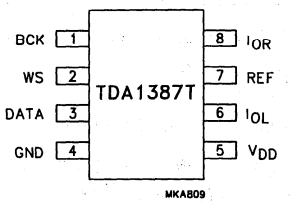


Fig.2 Pin configuration.

Bitstream continuous calibration filter-DAC for CD-ROM audio applications

TDA1388

FEATURES

Multiple format input interface

- I^2S-bus and LSB-justified input format compatible
- $1f_s$ input format data rate.

Extensive channel manipulation features

- Separate soft mute on left and right channel
- Channel interchange function (left to right and right to left)
- Monaural function (left to right or right to left)
- True mono function ½(left plus right).

Digital sound processing

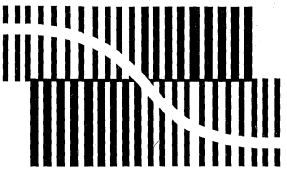
- Separate digital volume control for left and right channels
- Digital tone control, bass boost and treble
- dB-linear volume and tone control (low microcontroller load)
- Digital de-emphasis
- Soft mute.

Advanced audio output configuration

- Stereo line output (under microcontroller volume control)
- Stereo headphone output (under 5-tap potentiometer volume control)
- Line output independent of headphone output volume
- Power on/off click prevention circuitry
- High linearity, dynamic range, low distortion.

General

- Integrated digital filter plus DAC plus headphone driver
- No analog post filter required
- Easy application
- Functions controllable by static pins or by microcontroller interface
- 5 V power supply
- Low power consumption
- Small package size (SO28 and SSOP28).



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1388 CMOS digital-to-analog bitstream converter incorporates an up-sampling digital filter and noise shaper, unique signal processing features and integrated line and headphone drivers. The digital processing features are of high sound quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1388 supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB justified serial data input format with word lengths of 16, 18 and 20 bits. Two cascaded half-band filters and a sample-and-hold function increase the oversampling rate from $1f_s$ to $64f_s$. A 2nd-order noise shaper converts this oversampled data to a bitstream for the 5-bit continuous calibration Digital-to-Analog Converters (DACs).

On board amplifiers convert the output current to a voltage signal capable of driving a line output. The signal is also used to feed the integrated headphone amplifiers. The volume of the headphone is controlled by an external potentiometer.

The TDA1388 has special sound processing features for use in CD-ROM audio applications, which can be controlled by static pins or microcontroller interface. These functions are de-emphasis, volume, bass boost, treble, soft mute and the channel manipulation functions needed for ATAPI-compliant functionality in CD-ROM audio processing.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1388T	SO28	plastic small outline package; 28 leads; body width 7.5 mm.	SOT136-1
TDA1388M	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm.	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	note 1	4.5	5.0	5.5	V
I_{DD}	supply current	note 2	–	22	–	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 5 V	0.9	1.0	1.1	V
(THD+N)/S	total harmonic distortion plus noise as a function of signal for the line output	0 dB signal; R_L = 5 kΩ	–	–85	–80	dB
			–	0.006	0.013	%
		–60 dB signal; R_L = 5 kΩ	–	–35	–30	dBA
			–	1.8	3.2	%
	total harmonic distortion plus noise as a function of signal for the headphone output	0 dB signal; R_L = 16 Ω	–	–65	–	dB
			–	0.056	–	%
		0 dB signal; R_L = 32 Ω	–	–70	–	dB
			–	0.032	–	%
		–60 dB signal; R_L = 16 Ω or R_L = 32 Ω	–	–35	–30	dBA
			–	1.8	3.2	%
S/N	signal-to-noise ratio	A-weighted; at code 00000H	90	95	–	dBA
BR	input bit rate at data input	$f_{sys} = 256f_s$	–	$64f_s$	–	bits
		$f_{sys} = 384f_s$	–	$48f_s$	–	bits
f_{sys}	system clock frequency		8.192	–	18.432	MHz
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 5 V.

BLOCK DIAGRAM

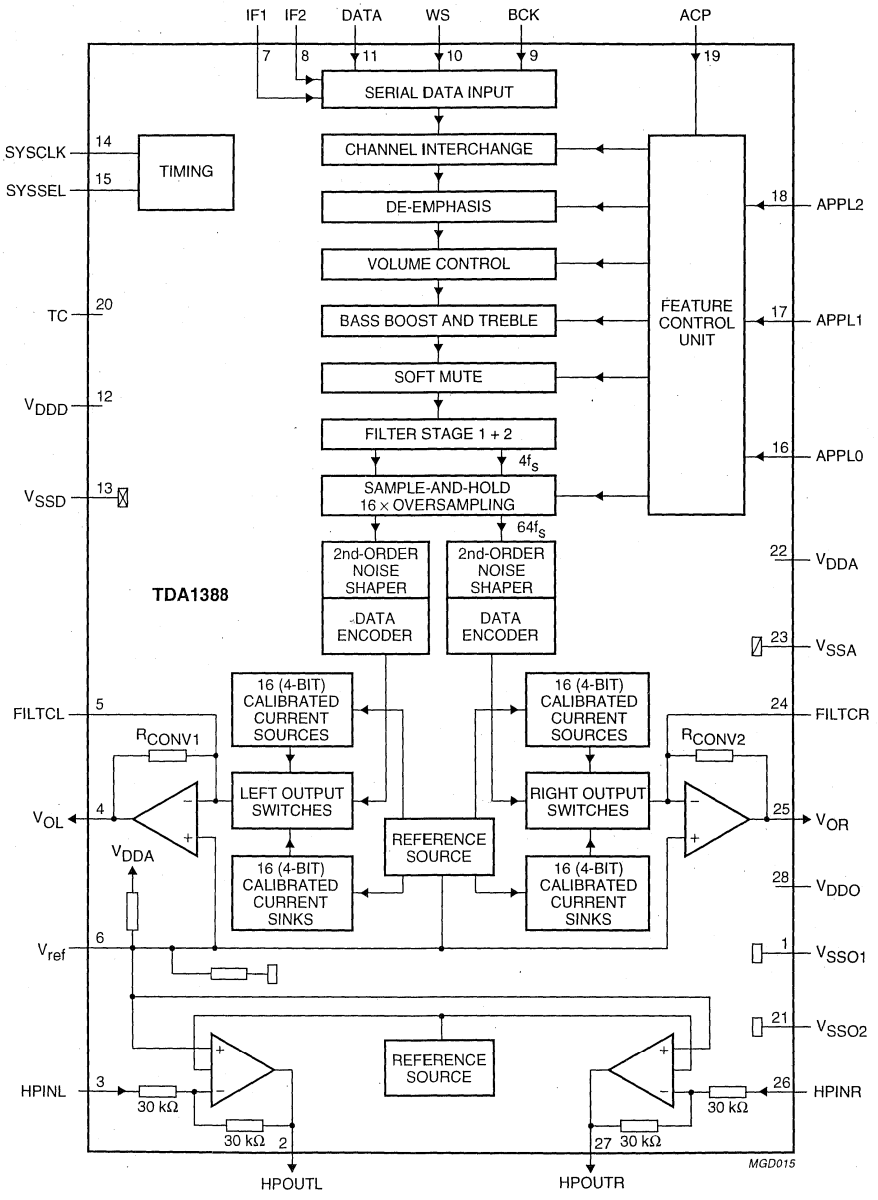


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSO1}	1	operational amplifier ground 1
HPOUTL	2	left headphone output voltage
HPINL	3	left headphone input voltage
V_{OL}	4	left channel audio voltage output
FILTCL	5	capacitor for left channel 1st-order filter function, should be connected between this pin and V_{OL} (pin 4)
V_{ref}	6	internal reference voltage
IF1	7	input format selection 1
IF2	8	input format selection 2
BCK	9	bit clock input
WS	10	word selection input
DATA	11	data input
V_{DDD}	12	digital supply voltage
V_{SSD}	13	digital ground
SYSCLK	14	system clock $256f_s$ or $384f_s$
SYSSEL	15	system clock selection
APPL0	16	application mode 0 input
APPL1	17	application mode 1 input
APPL2	18	application mode 2 input
ACP	19	application control input
TC	20	test control
V_{SSO2}	21	operational amplifier ground 2
V_{DDA}	22	analog supply voltage
V_{SSA}	23	analog ground
FILTCR	24	capacitor for right channel 1st-order filter function, should be connected between this pin and V_{OR} (pin 25)
V_{OR}	25	right channel audio voltage output
HPINR	26	right headphone input voltage
HPOUTR	27	right headphone output voltage
V_{DDO}	28	operational amplifier supply voltage

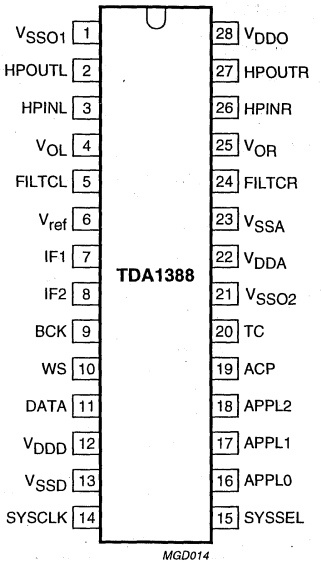


Fig.2 Pin configuration.

2 × 6 W stereo car radio power amplifier — TDA1517

FEATURES

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- Load dump protection
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Electrostatic discharge protection
- Compatible with TDA1519 (except gain).

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin; 9 leads (SIL9MPF) and a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for car radio and multi-media applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage					
	operating		6.0	14.4	18.0	V
	non-operating		–	–	30.0	V
	load dump protected		–	–	45.0	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		50	–	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 0.5%	–	5	–	W
		R_L = 4 Ω; THD = 10%	–	6	–	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz	48	–	–	dB
α_{cs}	channel separation		40	–	–	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		–	50	–	μV
T_c	crystal temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA1517P	HDIP18	plastic heat-dissipating dual in-line; 18 leads	SOT398-1

BLOCK DIAGRAM

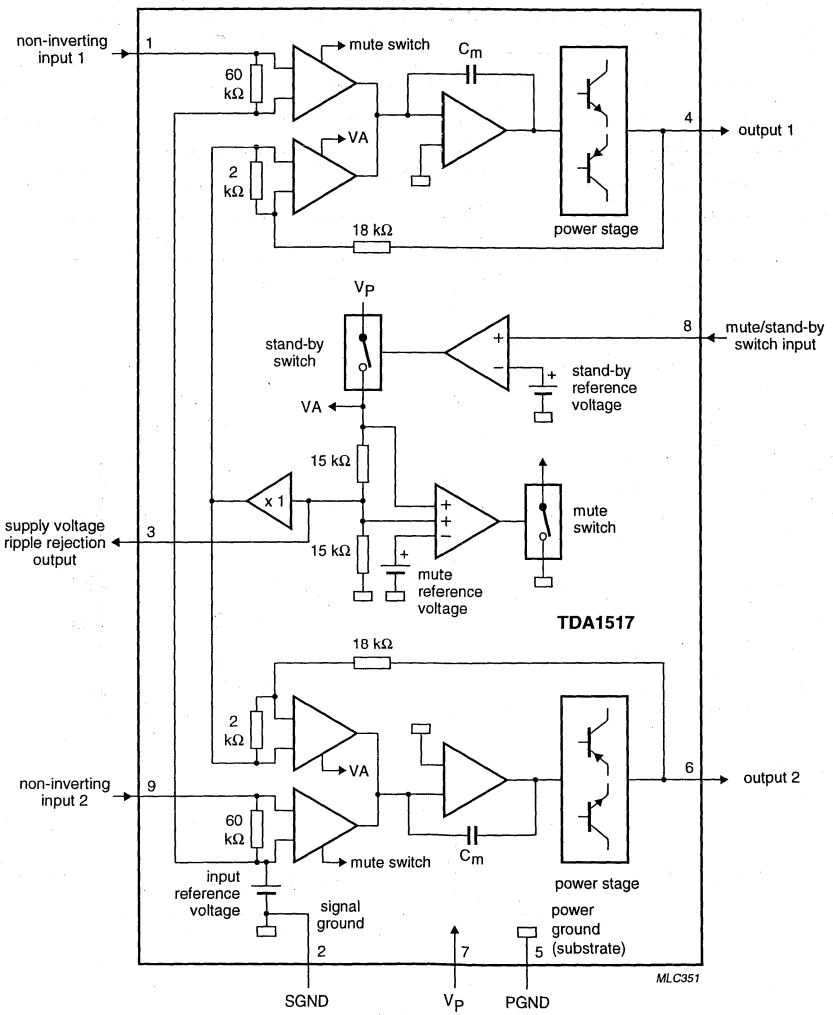


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V_P	7	supply voltage
M/SS	8	mute/standby switch input
–INV2	9	non-inverting input 2

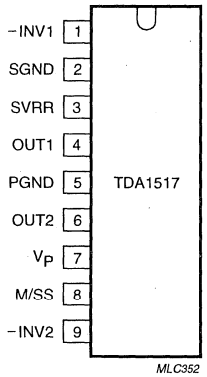
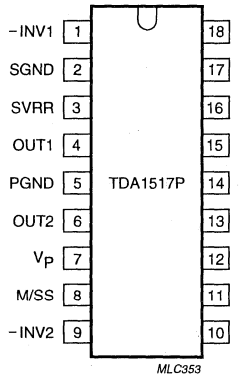


Fig.2 Pin configuration for SOT110-1.



Pins 10 to 18 connected to GND or floating.

Fig.3 Pin configuration for SOT398-1.

Stereo cassette head preamplifier and equalizer

TDA1522

FEATURES

- Two independent amplifiers with open-loop gain of 90 dB (typical)
- Internal DC feedback via 140 kΩ resistor from output to feedback point
- AC characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at DC ground that eliminates the input coupling capacitor
- Minimum external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- DC input current <2 μA
- Wide supply voltage range.

GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 8)		7.5	–	23	V
I_P	supply current (pin 8)		–	5	–	mA
T_{amb}	operating ambient temperature		−30	–	+85	°C
THD	total harmonic distortion		–	0.05	–	%
α_{cs}	channel separation	R_S = 10 kΩ; L_S = 0	45	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1522	SIL9MP	plastic single in-line medium power package; 9 leads	SOT142-1

BLOCK DIAGRAM

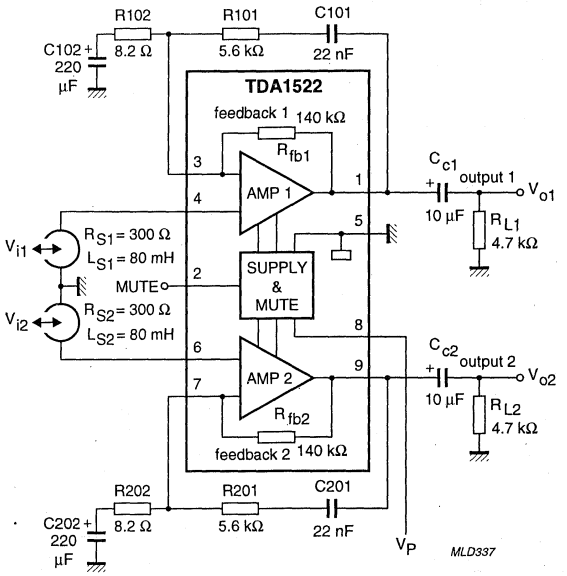


Fig.1 Block diagram with external components; also used as test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{o1}	1	output voltage 1
MUTE	2	mute input
FB1	3	feedback 1
V_{i1}	4	input voltage 1
GND	5	ground
V_{i2}	6	input voltage 2
FB2	7	feedback 2
V_P	8	power supply
V_{o2}	9	output voltage 2

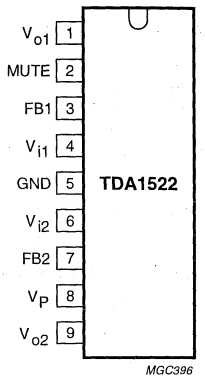


Fig.2 Pin configuration.

Stereo cassette head preamplifier and equalizer

TDA1523

FEATURES

- Two independent amplifiers with open-loop gain of 90 dB (typical)
- Internal DC feedback via 140 kΩ resistor from output to feedback point
- AC characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at DC ground that eliminates the input coupling capacitor
- Minimum external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- DC input current <2 μA.

GENERAL DESCRIPTION

The TDA1523 is a playback amplifier for car radio/cassette players.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)		7.5	–	12	V
I_P	supply current (pin 7)		–	5	–	mA
T_{amb}	operating ambient temperature		–30	–	+85	°C
THD	total harmonic distortion		–	0.05	–	%
α_{cs}	channel separation	R_S = 10 kΩ; L_S = 0	45	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1523	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1

BLOCK DIAGRAM

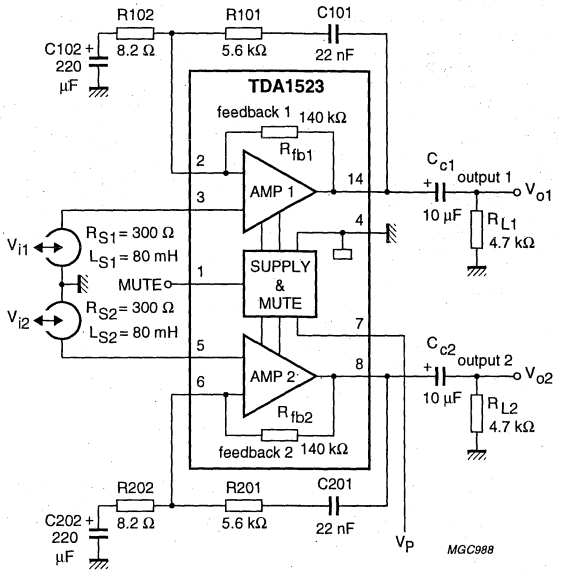


Fig.1 Block diagram with external components; also used as test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
MUTE	1	mute input
FB1	2	feedback 1
V_{i1}	3	input voltage 1
GND	4	ground
V_{i2}	5	input voltage 2
FB2	6	feedback 2
V_P	7	power supply
V_{o2}	8	output voltage 2
n.c.	9	not connected
n.c.	10	not connected
n.c.	11	not connected
n.c.	12	not connected
n.c.	13	not connected
V_{o1}	14	output voltage 1

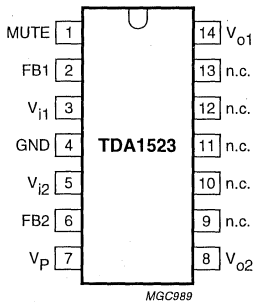


Fig.2 Pin configuration.

Bitstream Continuous Calibration DAC with digital sound processing (BCC-DAC)

TDA1546T

1 FEATURES

1.1 Easy application

- Voltage output 1.5 V (RMS)
- Operational amplifiers and cascaded 4-stage digital FIR filter integrated
- Master and slave mode clock system with selectable system clock (f_{sys}) $256f_s$ or $384f_s$
- I^2S-bus serial input format or Japanese 16, 18 or 20 bits serial input mode
- All features are accessible under remote control
- Simple 3-line serial microcontroller command interface
- Power-on reset
- 28 lead small outline package.

1.2 High performance

- Superior signal-to-noise ratio
- Low total harmonic distortion
- Wide dynamic range
- No zero crossing distortion
- Continuous calibration digital-to-analog conversion combined with noise shaping techniques
- Second-order noise shaper
- 128 times oversampling in normal-speed mode
- 64 times oversampling in double-speed mode.

1.3 Digital sound processing features

1.3.1 VOLUME CONTROL FEATURES

- Smoothed transitions before and after digital mute (soft mute)
- Fade function: duration-programmable (6 ms to 22.4 s at 44.1 kHz) digital volume control (attenuation as well as gain): +6 dB to −90 dB in steps of 0.375 dB with automatic soft mute
- Digital balance: 0 dB to −22.5 dB in steps of −1.5 dB (maximum overall attenuation combined with volume control: −90 dB)

1.3.2 SOUND PROCESSING FEATURES

- Digital de-emphasis filter for three sample rates (32 kHz, 44.1 kHz or 48 kHz)
- Digital treble: −10.5 dB to +12 dB at 20 kHz; 16 steps spaced at 1.5 dB
- Digital bass: −9 dB to +13.5 dB at 20 Hz; 16 steps spaced at 1.5 dB
- Distortion-free digital dynamic bass boost: 0 dB to +37 dB at 10 Hz; 15 steps spaced at 2 dB
- Can be used for loudness or dynamic digital bass boost
- Double-speed mode (e.g. for high-speed dubbing)
- Pseudo double-speed mode (for power saving application)
- Digital speaker system mode including digital crossover filter.

1.3.3 SOUND MONITOR FEATURES

- Spectrum analyzer for seven different frequency ranges
- Digital silence detection. Level (−48 dB to ∞ dB, in steps of 3 dB) and duration (200 ms to 3.2 s, in steps of 200 ms at 44.1 kHz) programmable. Output via versatile pins.
- Peak level detection and readout to microcontroller (dB linear, 0 dB to −90 dB in steps of 1.5 dB)
- Digital overload detection. Level-programmable (dB linear, −1.5 dB to −46.5 dB, in steps of 3 dB). Output via versatile pins.
- Digital spectrum analyzer by combination of peak detection and 7-band selective filter
- Optional combination spectrum analyzer and overload detection for frequency-dependent overload detection.

2 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1546T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

3 QUICK REFERENCE DATA

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	40	–	mA
I_{DDA}	analog supply current	note 2	–	5.5	–	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	–	mA
I_{DDX}	clock circuitry supply current	note 2	–	1	–	mA
$V_{FS(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 5 V	1.425	1.5	1.575	V
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–88	–81	dB
			–	0.004	0.009	%
		at –60 dB signal level; A-weighted	–	–44	–40	dB
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	108	–	dB
t_{dg}	group delay	f_s = sample rate; normal-speed	–	$\frac{24}{f_s}$	–	s
BR	input bit rate at data input	f_s = 48 kHz; normal-speed	–	–	3.072	Ms^{-1}
		f_s = 48 kHz; double-speed	–	–	6.144	Ms^{-1}
f_{sys}	system clock frequency		6.4	–	18.432	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (V_{OL} and V_{OR})		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 5 V.

4 GENERAL DESCRIPTION

The TDA1546T is the first Bitstream Continuous Calibration digital-to-analog converter (BCC-DAC) to feature unique signal processing functions. In addition to the basic functions of digital filtering and digital-to-analog conversion, it offers such advanced digital signal processing functions as volume control, tone control, bass boost, peak or spectrum analyzer readout and many more convenient functions. The digital processing features are of high sound quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1546T accepts I^2S-bus data input formats with word lengths of up to 20 bits and various Japanese serial data input formats with word lengths of 16, 18 and 20 bits. The circuit can operate as a master or slave with different system clocks ($256f_s$ or $384f_s$) and is therefore, eminently suitable for use in various applications such as DCC, CD, DAT and MD.

The range of applications is further extended by an incorporated Digital Speaker System mode (DSS) with digital crossover filter.

Four cascaded FIR filters and a sample-and-hold function increase the oversampling rate from $1f_s$ to $96f_s$ ($384f_s$ system clock) or $128f_s$ ($256f_s$ system clock). A second-order noise shaper converts this oversampled data to a bitstream for the 5-bit DACs.

The DACs are of the continuous calibration type and incorporate a special data coding technique, which contributes to a high signal-to-noise ratio and dynamic range.

On-board amplifiers convert the output current to a voltage signal capable of driving a line output. Externally connected capacitors perform the required first-order filtering. Additional post filtering is not required.

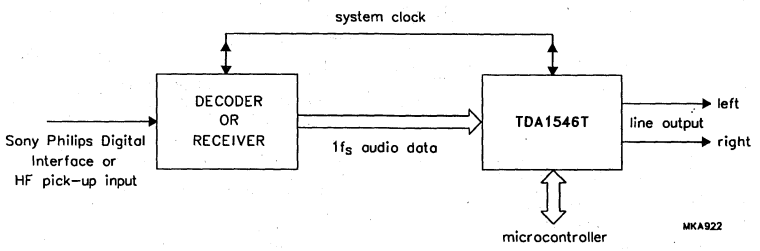


Fig.1 Digital audio reconstruction system using the TDA1546T.

5 BLOCK DIAGRAM

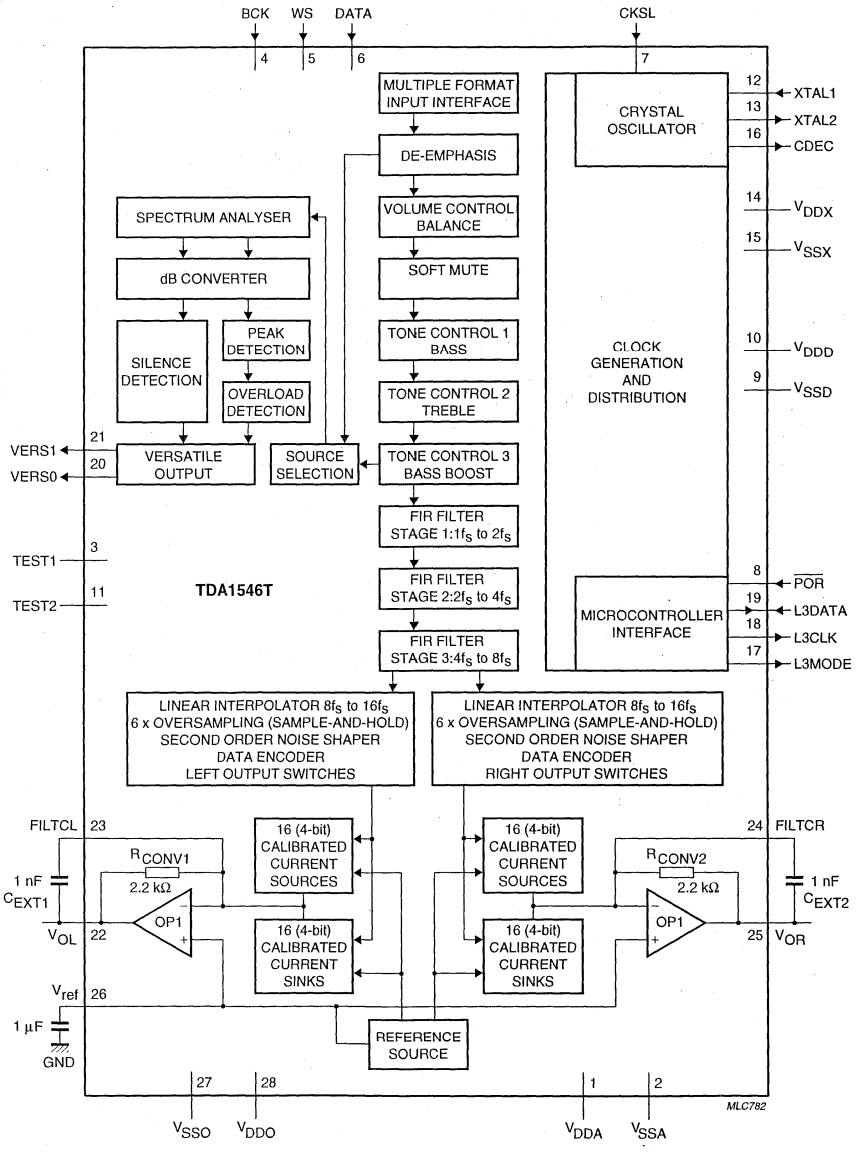


Fig.2 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
V_{DDA}	1	Analog supply voltage
V_{SSA}	2	Analog ground
TEST1	3	Test input 1. This pin should be connected to ground.
BCK	4	Bit clock input
WS	5	Word select input
DATA	6	Data input
CKSL	7	System clock frequency selection input
$\overline{POR}$	8	Power-on reset (active LOW). Internal pull-up resistor allows timed operation in combination with external capacitor.
V_{SSD}	9	Digital ground
V_{DDD}	10	Digital supply voltage
TEST2	11	Test input 2. This pin should be connected to ground.
XTAL1	12	Crystal oscillator input in master mode or external clock input in slave mode
XTAL2	13	Crystal oscillator drive output to crystal
V_{DDX}	14	Crystal oscillator supply voltage
V_{SSX}	15	Crystal oscillator ground
CDEC	16	System clock output
L3MODE	17	Identification of the L3-bus operation mode
L3CLK	18	Bit clock for synchronization of microcontroller data transfer
L3DATA	19	Bidirectional data line intended for control data from the microcontroller and peak data from the TDA1546T
VERS0	20	Versatile output 0 for silence or overload detection. Can be used to drive an LED.
VERS1	21	Versatile output 1 for silence or overload detection. Can be used to drive an LED.
V_{OL}	22	Left channel audio voltage output
FILTCL	23	Capacitor for left channel first-order filter function should be connected between this pin and V_{OL} (pin 22).
FILTCR	24	Capacitor for right channel first-order filter function should be connected between this pin and V_{OR} (pin 25).
V_{OR}	25	Right channel audio voltage output
V_{ref}	26	Decoupling pin for internal reference voltage, $\frac{1}{2}V_{DDA}$ (typ)
V_{SSO}	27	Internal operational amplifier ground
V_{DDO}	28	Internal operational amplifier supply voltage

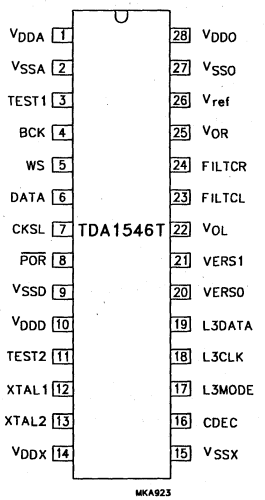


Fig.3 Pin configuration.

Bitstream continuous calibration filter-DAC with headphone driver and DSP

TDA1548T

FEATURESPRODUCT SPECIFICATION

Easy application

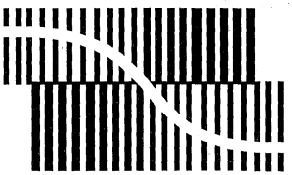
- Only first-order analog post-filtering required
- Headphone amplifiers and digital filter integrated
- Component saving common headphone output
- Selectable system clock (SYSCLK) $64f_s$, $256f_s$ or $384f_s$
- 16, 18 or 20 bits I^2S-bus or LSB justified serial input format
- Input pins suitable with 5 V low supply voltage interfacing
- Small package (SSOP28)
- Single rail supply (3 V).

High performance

- Superior signal-to-noise ratio
- Wide dynamic range
- Continuous calibration digital-to-analog conversion combined with noise shaping technique.

Features

- Low power dissipation
- Digital volume control
- Soft mute
- Digital tone control (Bass Boost and Treble)
- Digital de-emphasis
- Analog control of digital sound control functions.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1548T is a dual CMOS digital-to-analog converter (DAC) with up-sampling filter and noise shaper and integrated headphone driver featuring unique signal processing functions. The digital processing features are of high sound processing quality due to the wide dynamic range of the bitstream conversion technique.

The TDA1548T supports the I^2S-bus data input mode with word lengths of up to 20 bits and the LSB justified serial data input format with word lengths of 16, 18 or 20 bits. The clock system is selectable ($64f_s$, $256f_s$ or $384f_s$) by means of selection pins. Two cascaded half band filters, linear interpolator and a sample-and-hold function increase the oversampling rate from $1f_s$ to $64f_s$.
A second-order noise shaper converts this oversampled data into a bitstream for the 5-bit continuous calibration DACs.

On board amplifiers convert the output current to a voltage signal capable of driving a headphone or line output.
The common operational amplifier application eliminates the need for capacitors.

The TDA1548T has some sound processing functions which are controllable by a potentiometer. These functions are volume, bass boost and treble. The flat/min/max switch can also be controlled by a potentiometer.
The analog values are converted to a digital code, which is then further translated internally to a set of coefficients for either volume, bass boost or treble.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1548T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA1548TZ	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.7	3.0	4.0	V
I_{DD}	supply current	note 2	–	15	–	mA
$V_{oFS(rms)}$	full-scale output voltage	V_{DD} = 3 V	0.57	0.64	0.71	V
(THD+N)/S	total harmonic distortion plus noise as a function of signal	0 dB signal	–	–65	–60	dB
			–	0.056	0.1	%
		0 dB signal; R_{OL} = 5 kΩ	–	–85	–78	dB
			–	0.006	0.013	%
		–60 dB signal; R_{OL} = 32 Ω or R_{OL} = 5 kΩ	–	–35	–30	dBA
			–	1.778	3.162	%
S/N	signal-to-noise ratio	A-weighted; at code 00000H	90	95	–	dBA
BR	input bit rate at data input	$f_{sys} = 384f_s$	–	$48f_s$	–	
		$f_{sys} = 256f_s$	–	$64f_s$	–	
		$f_{sys} = 64f_s$	–	$64f_s$	–	
f_{sys}	system clock frequency		2.048	–	18.432	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–20	–	+70	°C

Notes

1. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. Measured at input code 00000H and V_{DD} = 3 V.

BLOCK DIAGRAM

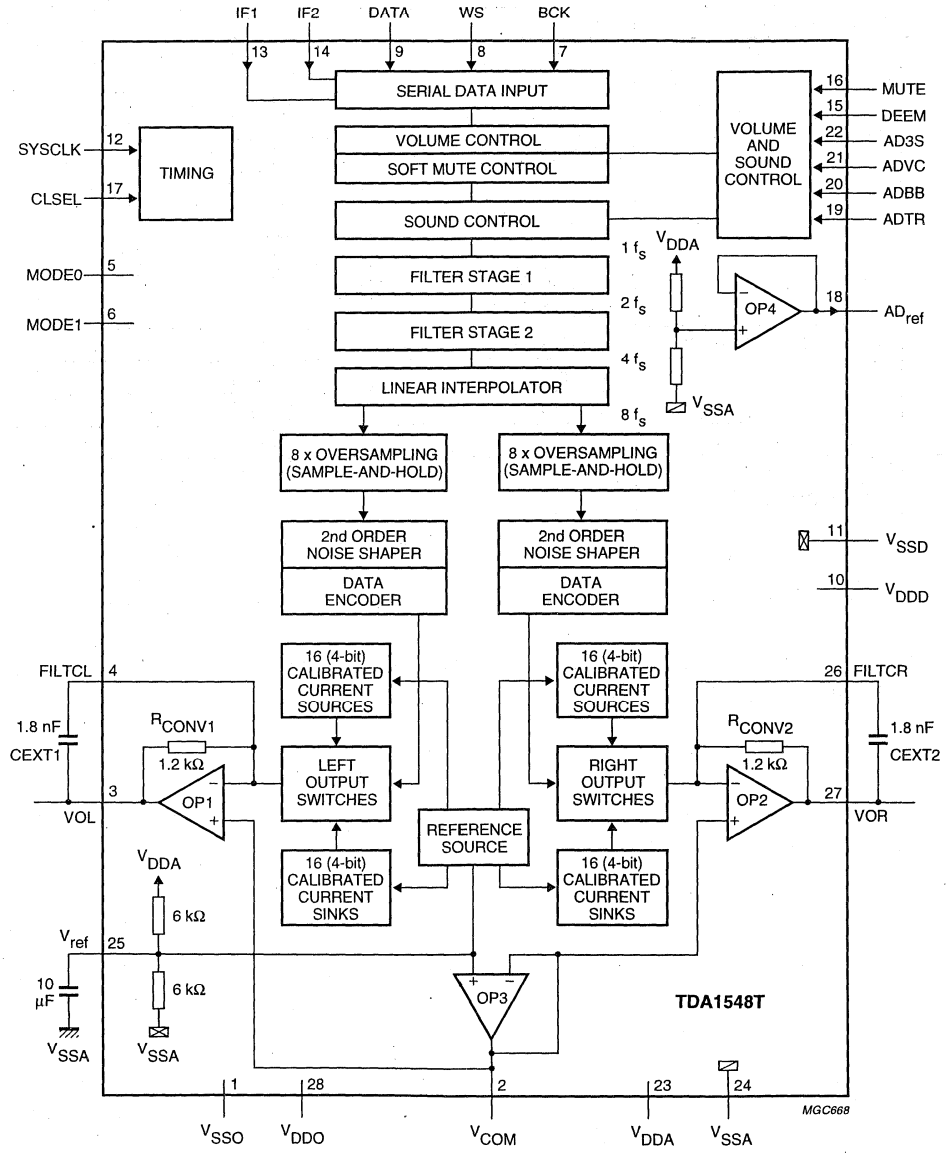


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSO}	1	operational amplifier ground
V_{COM}	2	common output pin
VOL	3	left channel audio voltage output
FILTCL	4	capacitor for left channel first-order filter function should be connected between this pin and VOL (pin 3)
MODE0	5	mode 0 selection pin
MODE1	6	mode 1 selection pin
BCK	7	bit clock input
WS	8	word select input
DATA	9	data input
V_{DDD}	10	digital supply voltage
V_{SSD}	11	digital ground
SYSCLK	12	system clock $64f_s$, $256f_s$ or $384f_s$
IF1	13	input format selection 1
IF2	14	input format selection 2
DEEM	15	de-emphasis input (f_s = 44.1 kHz) (active HIGH)
MUTE	16	soft-mute input (active HIGH)
CLSEL	17	system clock selection input
AD_{ref}	18	reference voltage output to external potentiometer
ADTR	19	analog sense input for treble setting
ADBB	20	analog sense input for bass boost setting
ADVC	21	analog sense input for volume control setting
AD3S	22	3-position switch input for flat/min/max setting
V_{DDA}	23	analog supply voltage
V_{SSA}	24	analog ground
V_{ref}	25	internal reference voltage ($0.5V_{DDA}$ typ)
FILTCR	26	capacitor for right channel first-order filter function should be connected between this pin and VOR (pin 27)
VOR	27	right channel audio voltage output
V_{DDO}	28	operational amplifier supply voltage

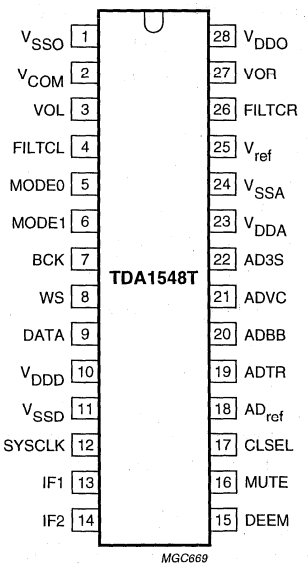


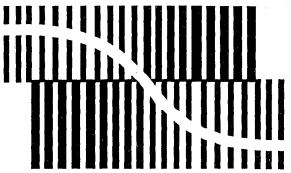
Fig.2 Pin configuration.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

FEATURES

- Easy application
- Finite-duration impulse-response (FIR) filtering and noise shaping incorporated
- 2nd-order noise shaper
- Wide dynamic range (true 18-bit resolution)
- Low total harmonic distortion
- No zero-crossing distortion
- Superior signal-to-noise ratio
- Bitstream continuous calibration conversion concept
- Inherently monotonic
- Voltage output (1.5 V RMS) at line drive level
- Single supply rail (3.8 to 5.5 V)
- Optimum output voltage level over the entire supply range
- Small outline packaging (SO16)
- Wide operating temperature range (–30 to +85 °C)
- Standard Japanese input format
- No analog post-filtering required
- Low power consumption
- Integrated operational amplifiers.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The TDA1549T (BCC-DAC1) is the first of a new generation of digital-to-analog converters featuring a unique combination of bitstream and continuous calibration concepts.

A system of digital filtering, high oversampling, 2nd order noise shaping and continuous calibration digital-to-analog conversion ensures that only simple 1st order analog filtering is required. The circuit accepts 18-bit four times oversampled input data ($4f_s$) in standard Japanese format. Internal FIR filters remove the main spectral components and increase the sampling rate to 96 times ($96f_s$). A 2nd order noise shaper converts this oversampled data to a 5-bit data stream. For low signal levels the converter operates in the 1-bit bitstream mode with attendant high differential linearity. Higher level signals are reproduced using the dynamic continuous calibration technique, thereby guaranteeing high linearity independent of process variations, temperature effects and product ageing.

High-precision, low-noise amplifiers convert the digital-to-analog current to an output voltage capable of driving a line output. Externally connected capacitors perform the required 1st order filtering so that no further post-filtering is required.

Internal reference circuitry ensures that the output voltage is proportional to the supply voltage, thereby making optimum use of the supply voltage over a wide range (3.8 to 5.5 V). This unique configuration of bitstream and continuous calibration techniques, together with a high degree of analog and digital integration, results in a digital-to-analog conversion system with true 18-bit dynamic range, high linearity and simple low-cost application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1549T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162–1

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

TDA1549T

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	3.8	5.0	5.5	V
V_{DDA}	analog supply voltage	note 1	3.8	5.0	5.5	V
V_{DDO}	operational amplifier supply voltage	note 1	3.8	5.0	5.5	V
I_{DDD}	digital supply current	note 2	–	12	18	mA
I_{DDA}	analog supply current	note 2	–	5.5	8	mA
I_{DDO}	operational amplifier supply current	note 2	–	6.5	9	mA
P_{tot}	total power dissipation	note 2	–	120	185	mW
		note 3	–	50	–	mW
$V_{FS(rms)}$	full-scale output voltage (RMS value)	$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V	1.425	1.500	1.575	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–90	–83	dB
			–	0.003	0.007	%
		at –60 dB signal level	–	–48	–40	dB
			–	0.40	1.0	%
		at –60 dB signal level; A-weighted	–	–50	–	dB
			–	0.38	–	%
S/N	signal-to-noise ratio at bipolar zero	A-weighted; at code 00000H	100	110	–	dB
t_{cs}	current setting time to ±1 LSB		–	0.1	–	µs
BR	input bit rate at data input		–	–	9.216	Mbits
f_{BCK}	input clock frequency		–	–	9.216	MHz
TC_{FS}	full-scale temperature coefficient at analog outputs (VOL and VOR)		–	$\pm 100 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–30	–	+85	°C

Notes

1. All V_{DD} and ground pins must be connected externally to the same supply.
2. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 5 V at input data code 00000H.
3. Measured with V_{DDD}, V_{DDA} and V_{DDO} = 3.8 V at input data code 00000H.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1)

BLOCK DIAGRAM

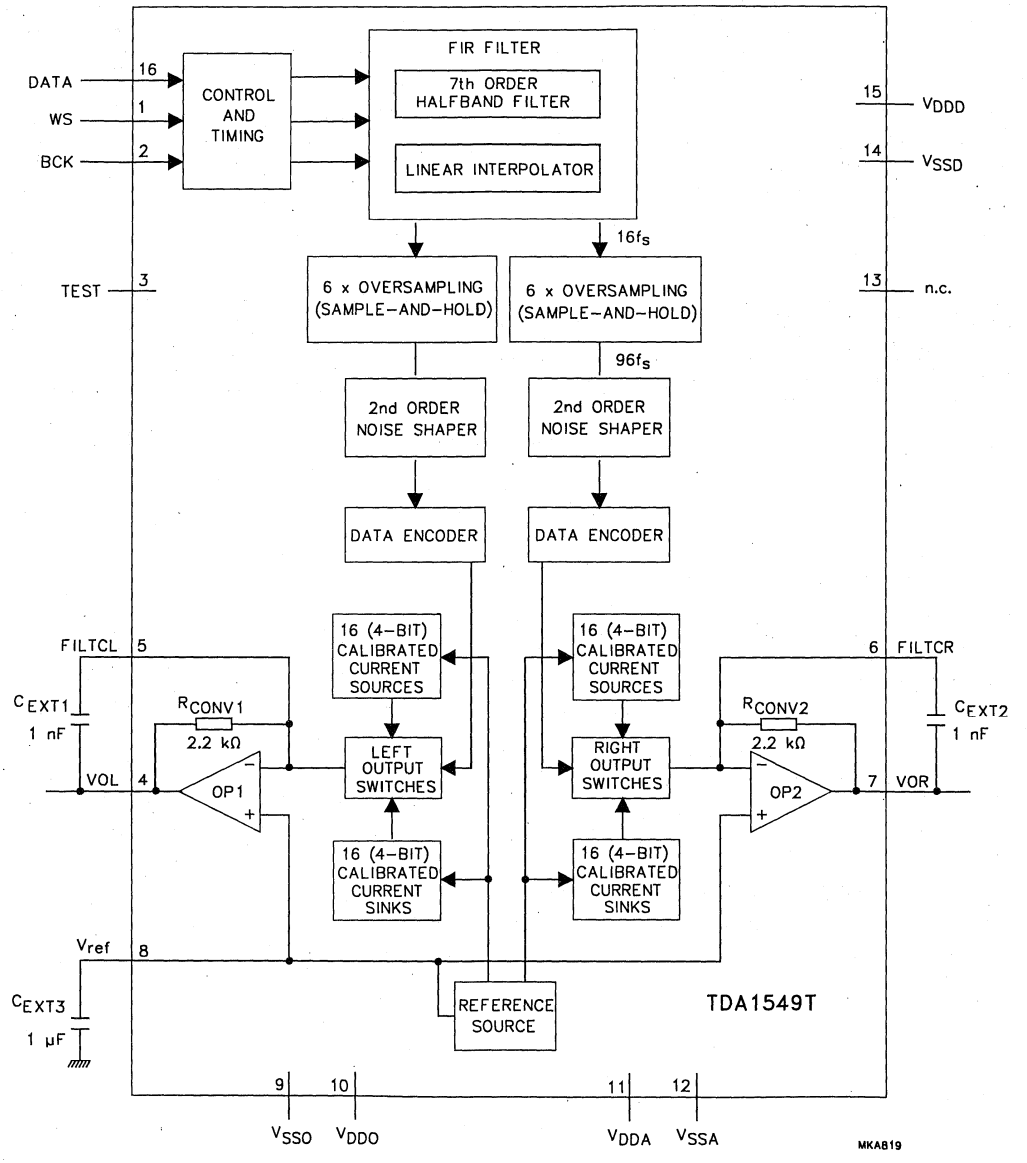


Fig.1 Block diagram.

Stereo $4f_s$ data input up-sampling filter with bitstream continuous calibration DAC (BCC-DAC1) TDA1549T

PINNING

SYMBOL	PIN	DESCRIPTION
WS	1	word select input
BCK	2	bit clock input
TEST	3	test input; pin should be connected to ground
VOL	4	left channel output
FILTCL	5	capacitor for left channel 1st order filter function; should be connected between pins 4 and 5
FILTCR	6	capacitor for right channel 1st order filter function; should be connected between pins 6 and 7
VOR	7	right channel output
V_{ref}	8	internal reference voltage for output channels ($\frac{1}{2}V_{DD}$)
V_{SSO}	9	operational amplifier ground
V_{DDO}	10	operational amplifier supply voltage
V_{DDA}	11	analog supply voltage
V_{SSA}	12	analog ground
n.c.	13	not connected (this pin should be left open-circuit)
V_{SSD}	14	digital ground
V_{DDD}	15	digital supply voltage
DATA	16	data input

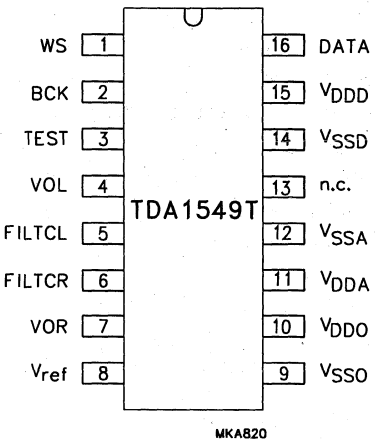


Fig.2 Pin configuration.

2 × 22 W stereo BTL car radio power amplifier with loudspeaker protection

TDA1553CQ

FEATURES

- Few peripheral components
- High output power
- Low output offset voltage
- Fixed gain
- Loudspeaker protection
- Good ripple rejection
- 3-state mode switch (operating, mute, standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Thermally protected
- Reverse polarity safe
- High energy handling capability at the outputs (V_P = 0)
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA1553CQ is a monolithic integrated class-B output amplifier in a 13-lead plastic DIL-bent-SIL power package. It contains 2 × 22 W amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage					
	operating		6	14.4	18	V
	non-operating		–	–	30	V
	load dump		–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_q	total quiescent current		–	80	–	mA
I_{stb}	standby current		–	40	100	μA
$\|Z_i\|$	input impedance		50	–	–	kΩ
T_{vj}	virtual junction temperature		–	–	150	°C
Stereo application						
P_O	output power	at 4 Ω; THD = 10%	–	22	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω; f = 100 Hz to 10 kHz	48	–	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
α_{cs}	channel separation		40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1553CQ	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

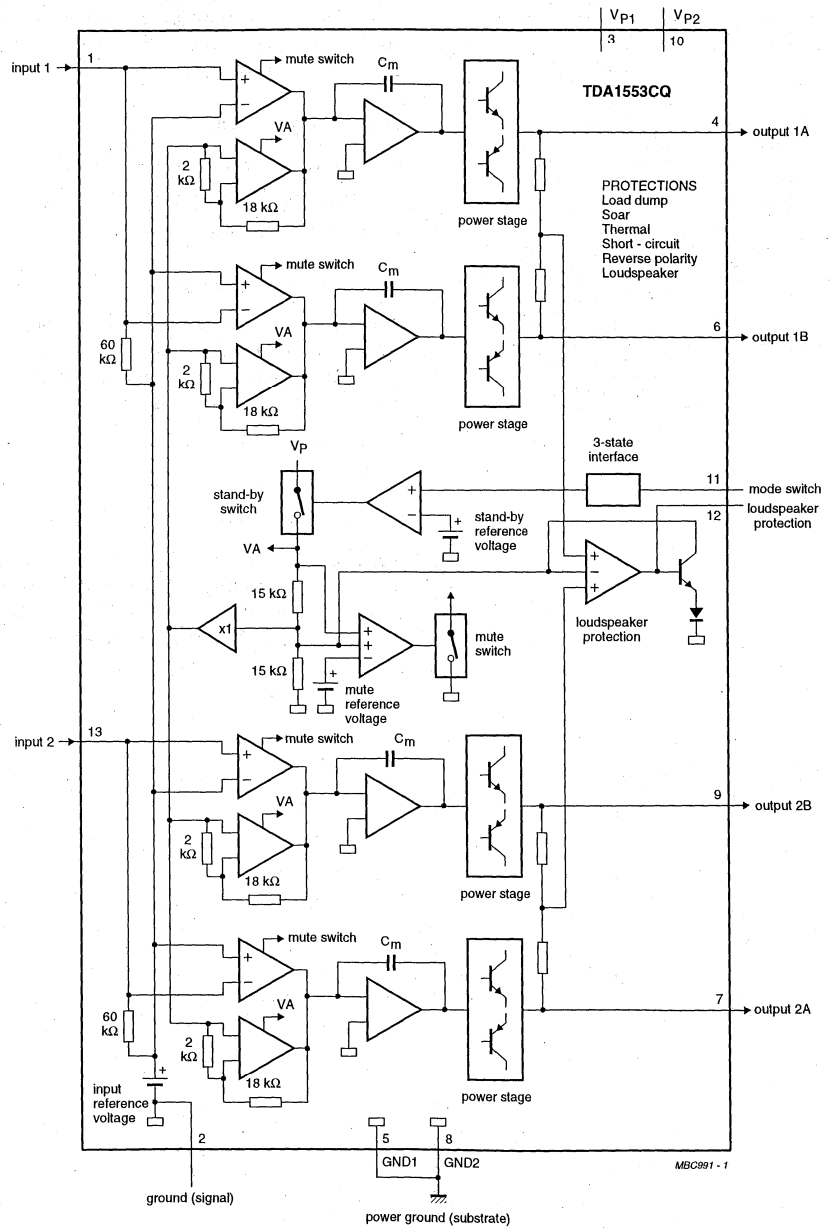


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage
OUT1A	4	output 1A
GND1	5	power ground 1
OUT1B	6	output 1B
OUT2A	7	output 2A
GND2	8	power ground 2
OUT2B	9	output 2B
V_{P2}	10	supply voltage
MODE	11	mode switch input
LSP	12	loudspeaker protection
IN2	13	input 2

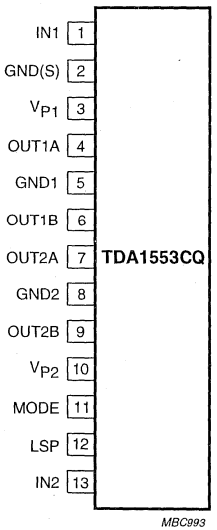


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1553CQ contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of the device are:

3-state mode switch

- standby: low supply current (<100 μA)
- mute: input signal suppressed
- operating: normal on condition.

Loudspeaker protection

When a short-circuit to ground occurs, which forces a DC voltage across the loudspeaker of ≥1 V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to ≤1 V.

Pin 12 detects the status of the protection circuit (e.g. for diagnostic purposes).

Short-circuit protection

If any output is short-circuited to ground during the standby mode, it becomes impossible to switch the circuit to the mute or operating condition. In this event the supply current will be limited to a few milliamps.

40 W car radio high power amplifier TDA1560Q

FEATURES

- Very high output power
- Low power dissipation when used for music signals
- Switches to low output power in the event of excessive heatsink temperatures
- Requires few external components
- Fixed gain
- Low cross-over distortion
- No switch-on/switch-off plops
- Mode select switch
- Low offset voltage at the output
- Load dump protection
- Short-circuit safe to ground, V_P and across load
- Protected against electrostatic discharge
- Thermally protected
- Diagnostic facility
- Flexible leads.

GENERAL DESCRIPTION

The TDA1560Q is an integrated Bridge-Tied Load (BTL) class-H high power amplifier. In a load of 8 Ω, the output power is 40 W typical at a THD of 10%.

The encapsulation is a 17-lead DIL-bent-SIL plastic power package. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	operating	8.0	14.4	18	V
		non-operating	–	–	30	V
		load dump protected	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	100	160	mA
I_{sb}	standby current		–	5	50	μA
G_v	voltage gain		29	30	31	dB
P_o	output power	R_L = 8 Ω; THD = 10%	–	40	–	W
		R_L = 8 Ω; THD = 0.5%	–	30	–	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz; R_S = 0 Ω	48	55	–	dB
V_{no}	noise output voltage		–	100	300	μV
$\|Z_i\|$	input impedance		180	300	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1560Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

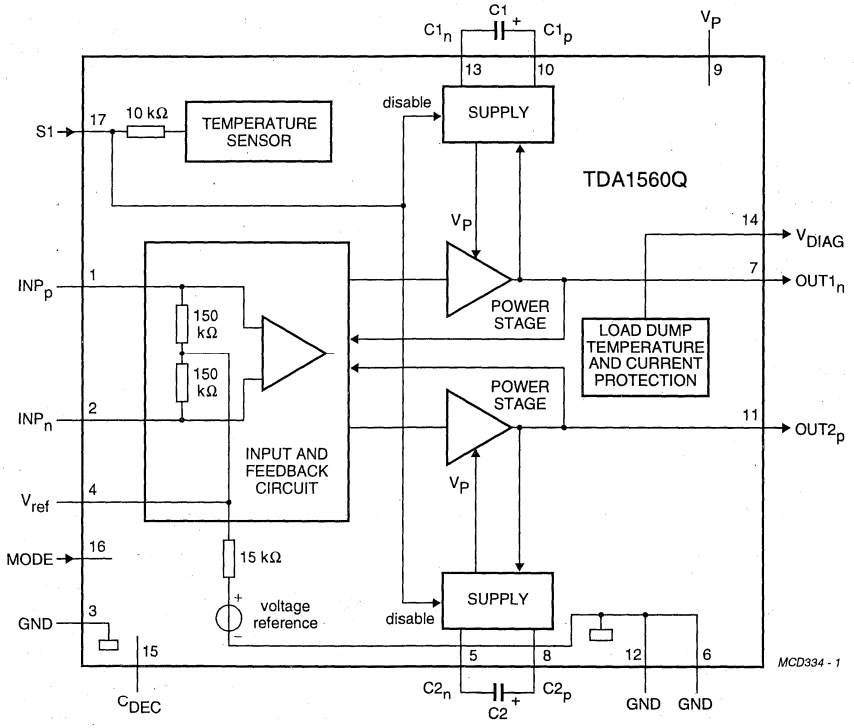


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INP_p	1	positive input
INP_n	2	negative input
GND	3	ground
V_{ref}	4	reference voltage
$C2_n$	5	capacitor C2 negative terminal
GND	6	ground
$OUT1_n$	7	output 1 (negative)
$C2_p$	8	capacitor C2 positive terminal
V_P	9	supply voltage
$C1_p$	10	capacitor C1 positive terminal
$OUT2_p$	11	output 2 (positive)
GND	12	ground
$C1_n$	13	capacitor C1 negative terminal
V_{DIAG}	14	diagnostic voltage output
C_{DEC}	15	decoupling
MODE	16	mode select switch input
S1	17	class-B/class-H input switch

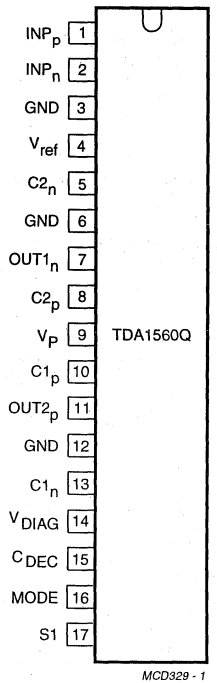


Fig.2 Pin configuration.

2 × 23 W car radio power amplifier TDA1561Q

FEATURES

- Low power dissipation due to switching from SE to BTL mode
- High common-mode rejection ratio (CMRR)
- Mute/standby/BTL-disable switch (mode select pin)
- Zero-crossing mute
- Load dump protection
- Short-circuit safe to ground, V_P and across load
- Loudspeaker protection
- Switches to single-ended operation at excessive crystal temperature.

GENERAL DESCRIPTION

The TDA1561Q is a monolithic power amplifier in a 13-lead plastic DIL-bent-SIL power package (DBS13P). It contains two identical 23 W amplifiers. The power dissipation is minimized by switching from single-ended (SE) to bridge-tied load (BTL) mode, when a higher output voltage swing is required. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	DC biased	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump protected	–	–	50	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	95	150	mA
I_{stb}	standby current		–	1	50	μA
$\lvert Z_I \rvert$	input impedance		–	60	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	21	23	–	W
G_v	closed loop voltage gain		31	32	33	dB
CMRR	common mode rejection ratio	f_i = 1 kHz; R_S = 0 Ω	–	80	–	dB
SVRR	supply voltage ripple rejection	f_i = 1 kHz; R_S = 0 Ω	45	55	–	dB
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	150	mV
α_{cs}	channel separation	R_S = 0 kΩ	40	–	–	dB
$\lvert \Delta G_v \rvert$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1561Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

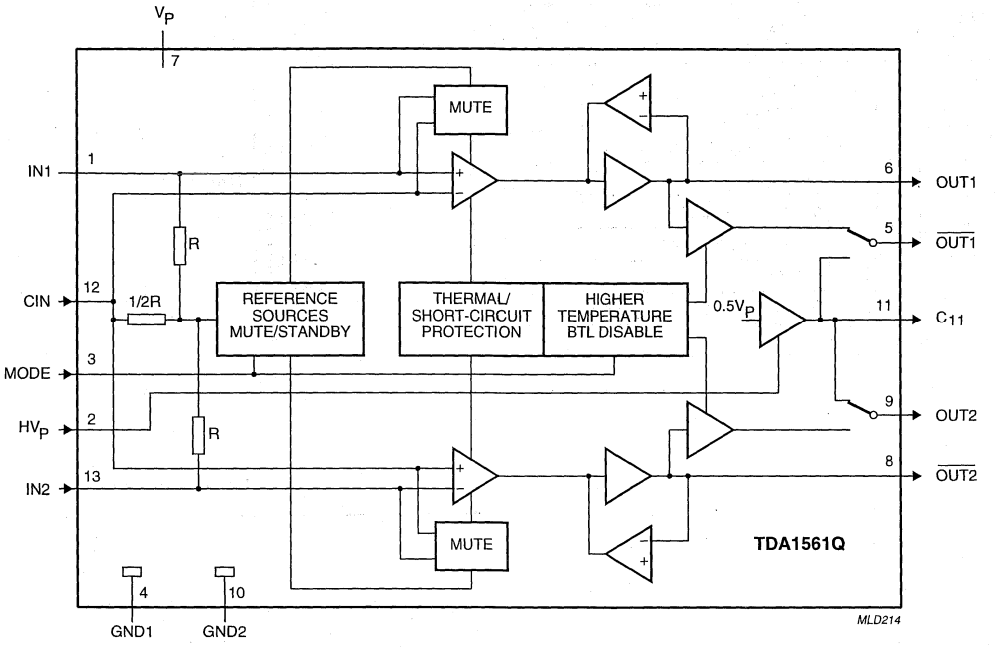


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
HV_P	2	half supply voltage control input
MODE	3	mute/standby/BTL-disable mode select switch input
GND1	4	ground 1
$\overline{OUT1}$	5	inverting output 1
OUT1	6	non-inverting output 1
V_P	7	supply voltage
$\overline{OUT2}$	8	inverting output 2
OUT2	9	non-inverting output 2
GND2	10	ground 2
C_{11}	11	single-ended electrolytic output
CIN	12	common input
IN2	13	input 2

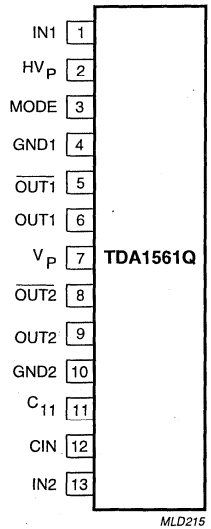


Fig.2 Pin configuration.

PLL stereo decoder and noise blanker TDA1592

FEATURES

- Adjustment-free voltage controlled PLL oscillator for ceramic resonator (f = 456 kHz)
- Pilot signal dependent mono/stereo switching
- Analog control of mono/stereo change over [stereo blend, Stereo Noise Controller (SNC)]
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis; High Cut Control (HCC)
- Reduced and controlled de-emphasis for AM operation (pin 7 to GND)
- Applicable as source selector for AM/FM/cassette switching
- Soft mute for silent tuning
- Separate interference noise detector
- Integrated input low-pass filter for delayed noise blanking
- Noise blanking at MPX-demodulator outputs.

GENERAL DESCRIPTION

The TDA1592 is a monolithic bipolar integrated circuit providing the stereo decoder function and noise blanking for FM car radio applications.

The device operates in a power supply range of 7.5 to 12 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 5)	7.5	10	12	V
I_P	supply current	–	15	20	mA
$V_{o(rms)}$	audio output signal (RMS value)	800	900	1000	mV
THD	total harmonic distortion	–	0.1	0.3	%
S/N	signal-to-noise ratio	–	82	–	dB
α_{cs}	channel separation	30	40	–	dB
V_{trigg}	interference voltage trigger level	–	10	–	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1592	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
TDA1592T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM

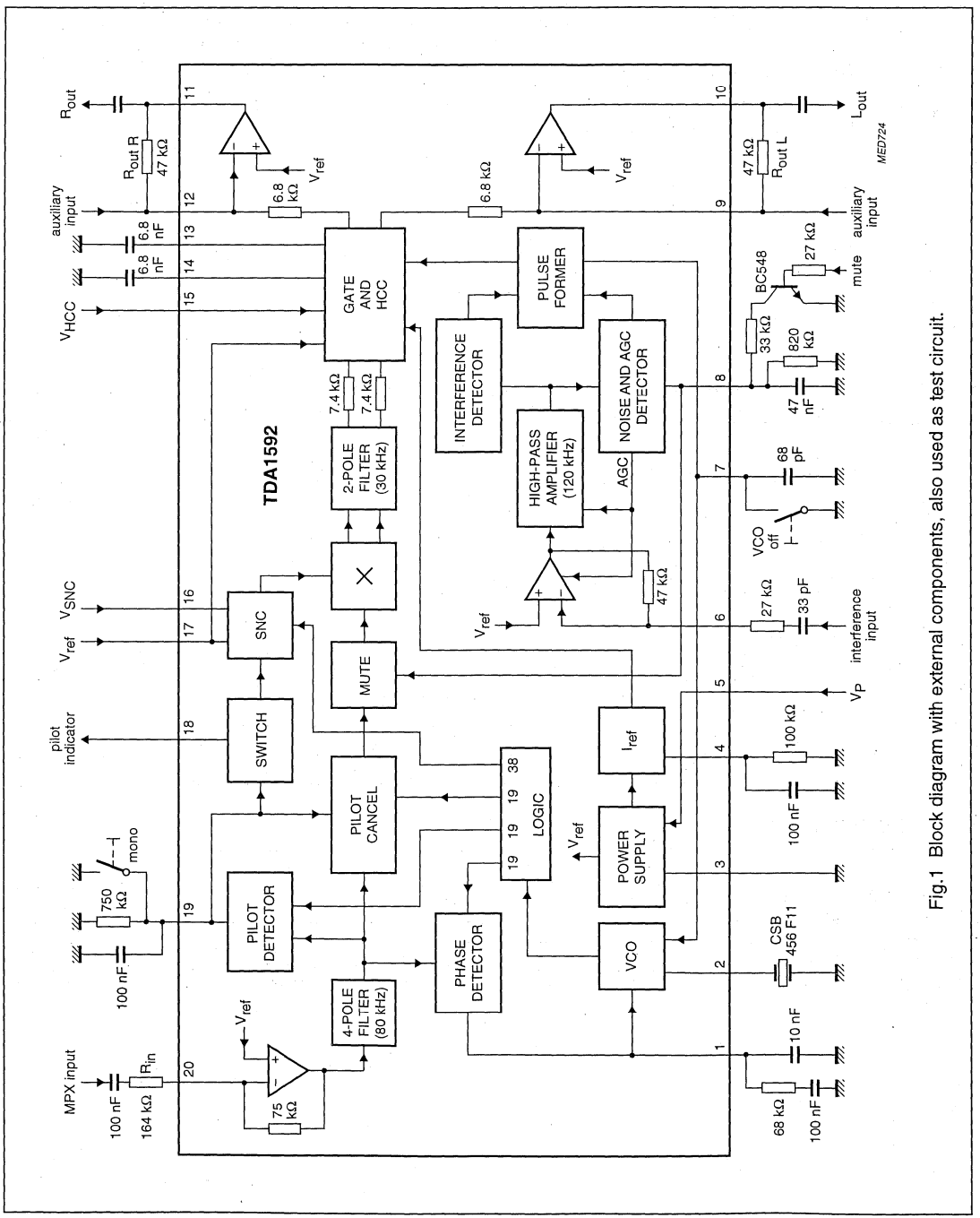


Fig.1 Block diagram with external components, also used as test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
PLL	1	phase locked loop filter
OSC	2	oscillator input/output pin for ceramic resonator
GND	3	ground (0 V)
I_{ref}	4	reference current
V_P	5	supply voltage (+10 V)
INFI	6	interference signal input
PUFO	7	pulse former time constant; VCO **off**
NDET	8	noise detector time constant; mute **on**
FB-L	9	AF feedback input for left audio signal
V_{oL}	10	AF output signal left
V_{oR}	11	AF output signal right
FB-R	12	AF feedback input for right audio signal
C_{DEEL}	13	de-emphasis capacitor for left channel
C_{DEER}	14	de-emphasis capacitor for right channel
HCC	15	HCC input for de-emphasis control
SNC	16	stereo blend input
V_{ref}	17	externally applied reference voltage of 1 to 5 V
IDENT	18	identification output (HIGH = pilot existing; stereo)
PILOT	19	pilot detector level (forced mono input)
$V_{i\,MPX}$	20	MPX input signal from IF demodulator

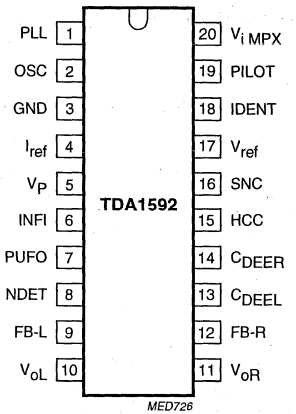


Fig.2 Pin configuration.

IF amplifier/demodulator for FM radio receivers

TDA1597

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1597 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; $\Delta f = \pm 75$ kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; $\Delta f = \pm 75$ kHz)	–	0.1	0.3	%
	with K2 adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature	−40	–	+85	°C

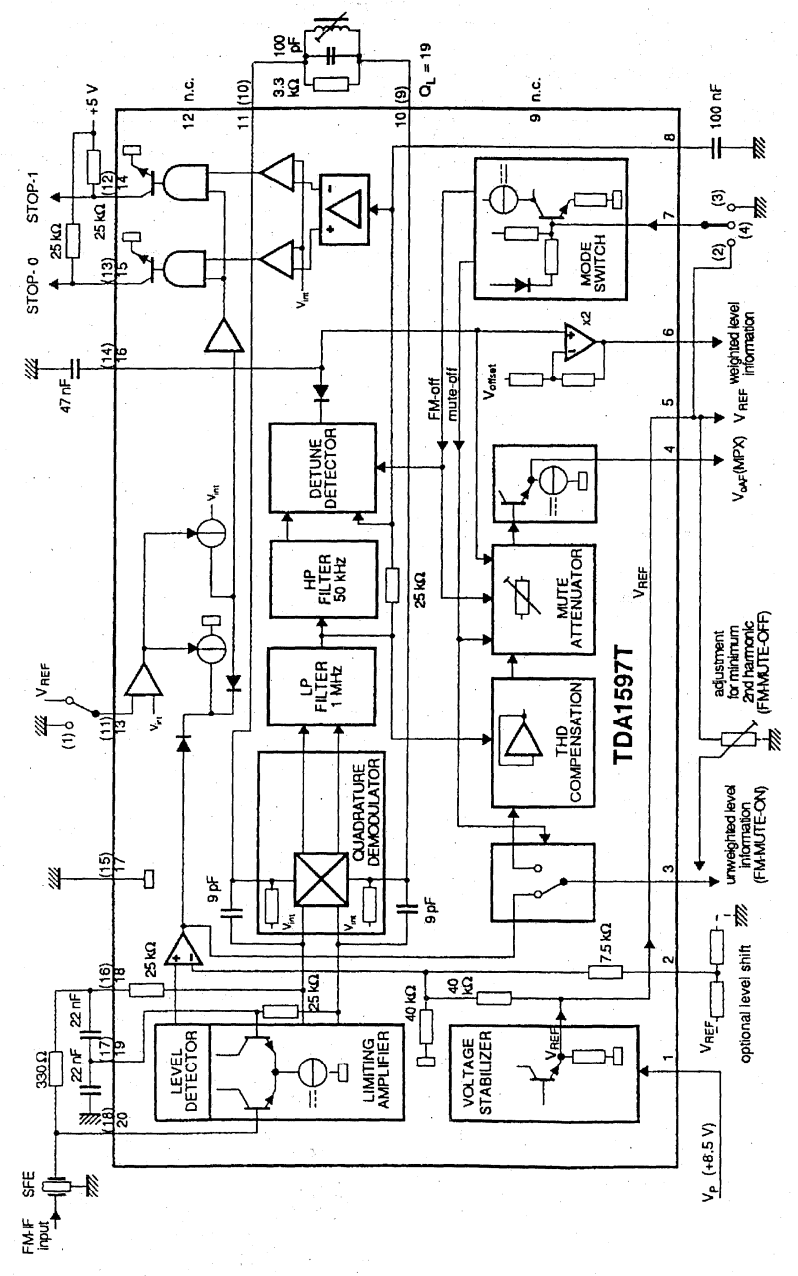
All pin numbers mentioned in this data sheet refer to the SO-version (TDA1597T) unless otherwise specified.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1597	18	DIL	plastic	SOT102(1)
TDA1597T	20	mini-pack	plastic	SOT163A(2)

Notes

1. SOT102-1; 1996 August 27.
2. SOT163-1; 1996 August 27.



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14)
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1597 pinning in parenthesis).

PINNING

(SO-version TDA1597T; pinning for DIL-version in parenthesis)

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output / K2 adjustment
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
MODE	7 (7)	mode switch input
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

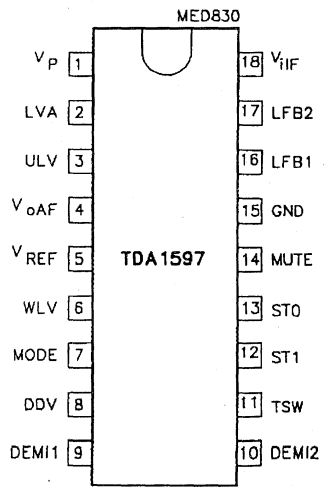


Fig.2 Pin configuration for DIL-version.

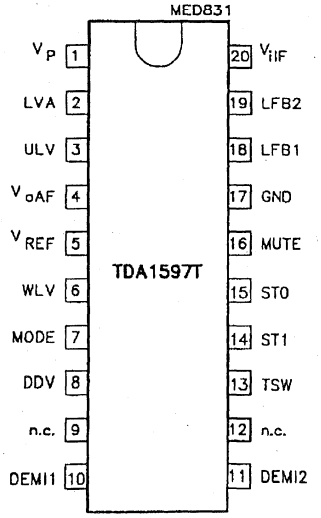


Fig.3 Pin configuration for SO-version.

IF amplifier/demodulator for FM radio receivers

TDA1599

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; $\Delta f = \pm 75$ kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; $\Delta f = \pm 75$ kHz)	–	0.1	0.3	%
	with K2 adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature	−40	–	+85	°C

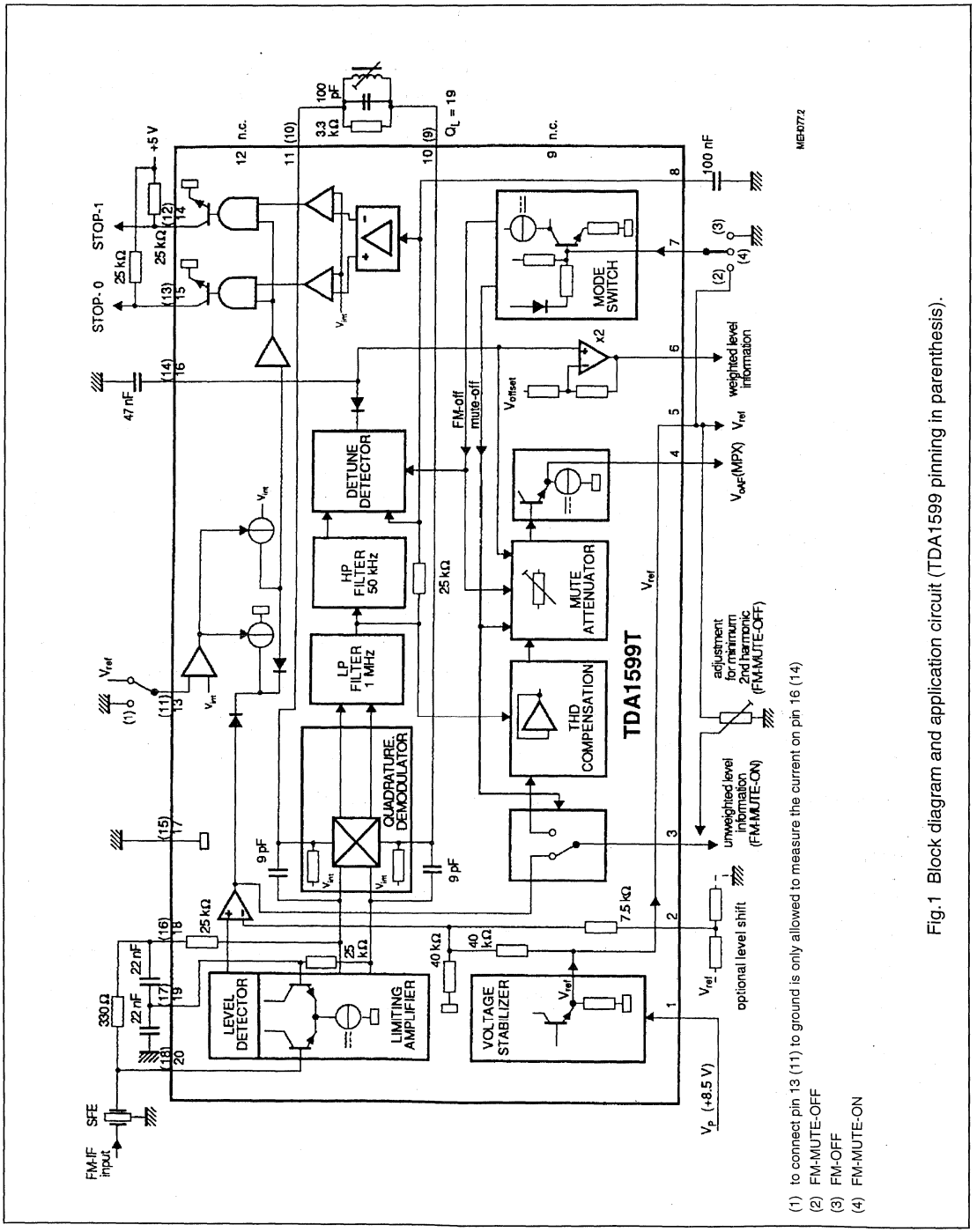
All pin numbers mentioned in this data sheet refer to the SO-version (TDA1599T) unless otherwise specified.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599	18	DIL	plastic	SOT102[1]
TDA1599T	20	mini-pack	plastic	SOT163A[2]

Notes

1. SOT102-1; 1996 August 29.
2. SOT163-1; 1996 August 29.



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14)
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1599 pinning in parenthesis).

PINNING; note 1

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output / K2 adjustment
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
MODE	7 (7)	mode switch input
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

Note

1. SO-version TDA1599T; pinning for DIL-version in parenthesis.

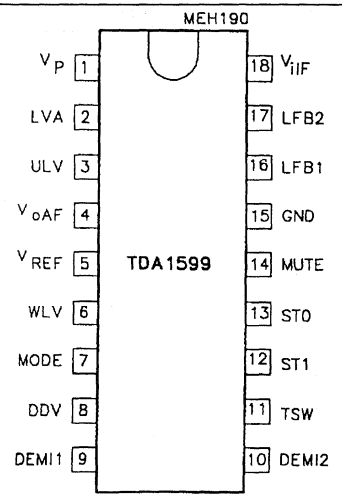


Fig.2 Pin configuration for DIL-version.

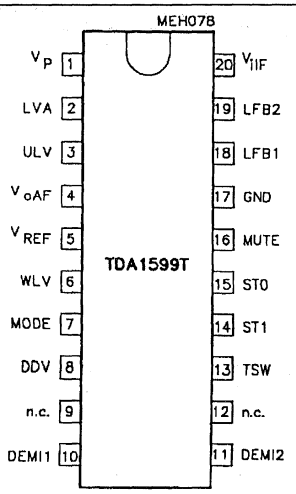


Fig.3 Pin configuration for SO-version.

2 × 6 W hi-fi audio power amplifier TDA2615

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-fi in accordance with *"IEC 268"* and *"DIN 45500"*
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2615 is a dual power amplifier in a 9-lead plastic single-in-line (SIL9MPF) medium power package. It has been especially designed for mains fed applications, such as stereo radio and stereo TV.

QUICK REFERENCE DATA

Stereo application.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\pm V_P$	supply voltage range		7.5	–	21	V
P_O	output power	$V_S = \pm 12$ V; THD = 0.5%	–	6	–	W
G_v	internal voltage gain		–	30	–	dB
$\lvert G_v \rvert$	channel unbalance		–	0.2	–	dB
α	channel separation		–	70	–	dB
SVRR	supply voltage ripple rejection		–	60	–	dB
V_{no}	noise output voltage		–	70	–	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA2615	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1

BLOCK DIAGRAM

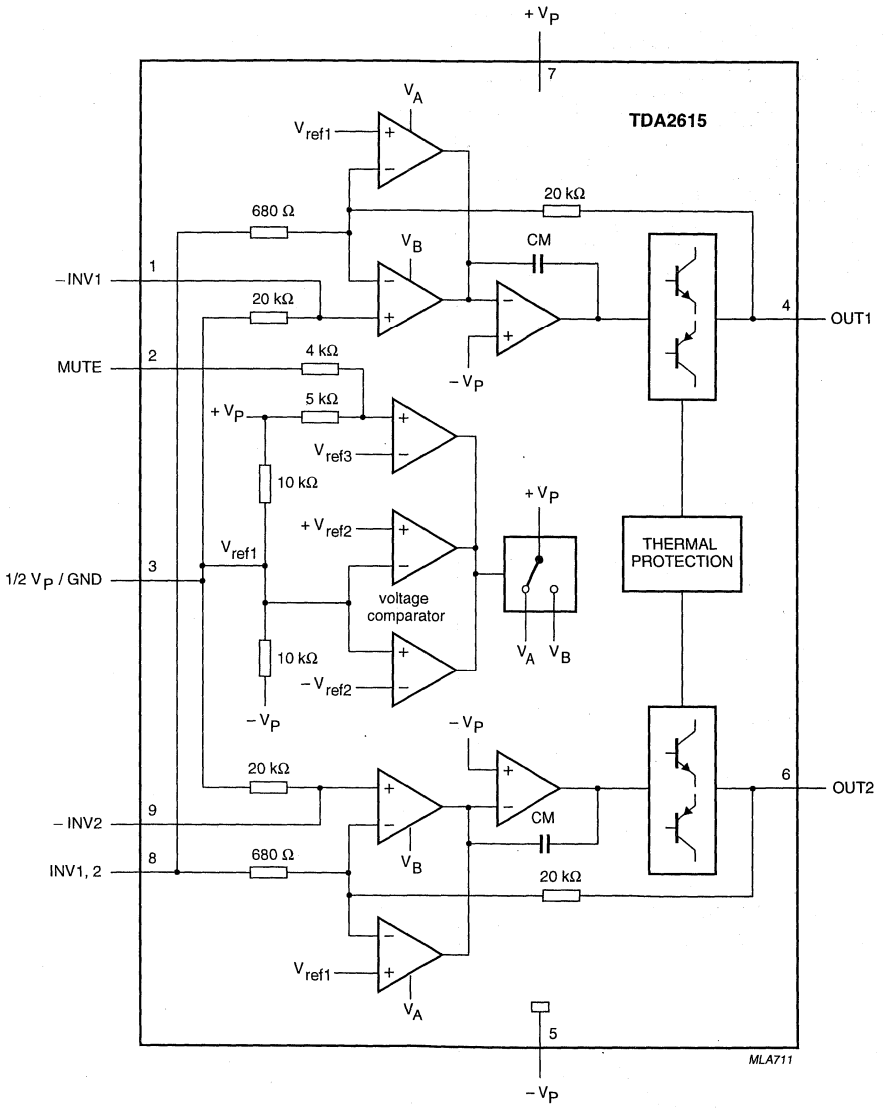


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
MUTE	2	mute input
½V_P/GND	3	½ supply voltage or ground
OUT1	4	output 1
–V_P	5	supply voltage (negative)
OUT2	6	output 2
+V_P	7	supply voltage (positive)
INV1, 2	8	inverting input 1 and 2
–INV2	9	non-inverting input 2

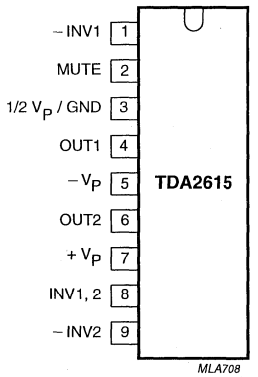


Fig.2 Pin configuration.

Multiple output voltage regulators

TDA3601Q
TDA3601AQ

FEATURES

- Six fixed voltage regulators
- Three microprocessor-controlled regulators
- Two V_P-state controlled regulators
- One fixed voltage regulator (can operate during load dump or thermal shutdown)
- V_{P1} supply pin (low current pin)
- V_{P2} supply pin (high current pin)
- RESET output (TDA3601Q) or $\overline{\text{RESET}}$ output (TDA3601AQ)
- Internally fixed timer of 100 µs
- Externally fixed delay timer
- High ripple rejection
- Flexible leads.

PROTECTION

- Current limit protection for regulator 1
- Foldback current limit protection (regulators 2 to 6)
- Load dump protection
- Thermal protection
- Regulator outputs DC short-circuit-safe to ground, V_P and other regulator outputs
- Capable of handling high energy on any of the output pins
- Reverse polarity safe.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Entire device						
V_{P1}	supply voltage range	operating	11	13.2	18	V
		load dump; notes 1 and 2	–	–	50	V
V_{P2}	supply voltage range	operating	11	13.2	18	V
		non-operating	–	–	30	V
		load dump; note 1	–	–	50	V
$I1_{tot}$	total quiescent current, V_{P1}	V_{P2} = 0; note 3	–	1	1.4	mA
T_c	crystal temperature		–	–	150	°C
Voltage regulators						
V_{R1}	output voltage regulator 1	0.5 mA ≤ I_{R1} ≤ 20 mA	4.75	5	5.25	V
V_{R2}	output voltage regulator 2	5 mA ≤ I_{R2} ≤ 200 mA	1.9	2.1	2.3	V
V_{R3}	output voltage regulator 3	5 mA ≤ I_{R3} ≤ 150 mA	4.75	5	5.25	V
V_{R4}	output voltage regulator 4	5 mA ≤ I_{R4} ≤ 150 mA	9	9.5	10	V
V_{R5}	output voltage regulator 5	5 mA ≤ I_{R5} ≤ 200 mA	9	9.5	10	V
V_{R6}	output voltage regulator 6	5 mA ≤ I_{R6} ≤ 200 mA	9.3	9.75	10.2	V

Notes

1. Load dump, during 50 ms, $t_r > 2.5$ ms.
2. Regulator 1 operating, 0.5 mA ≤ I_{R1} ≤ 20 mA.
3. V_{P1} = 13.2 V; V_{P2} = R4-sel = R5-sel = 0; I_{R1} = 0.

BLOCK DIAGRAM

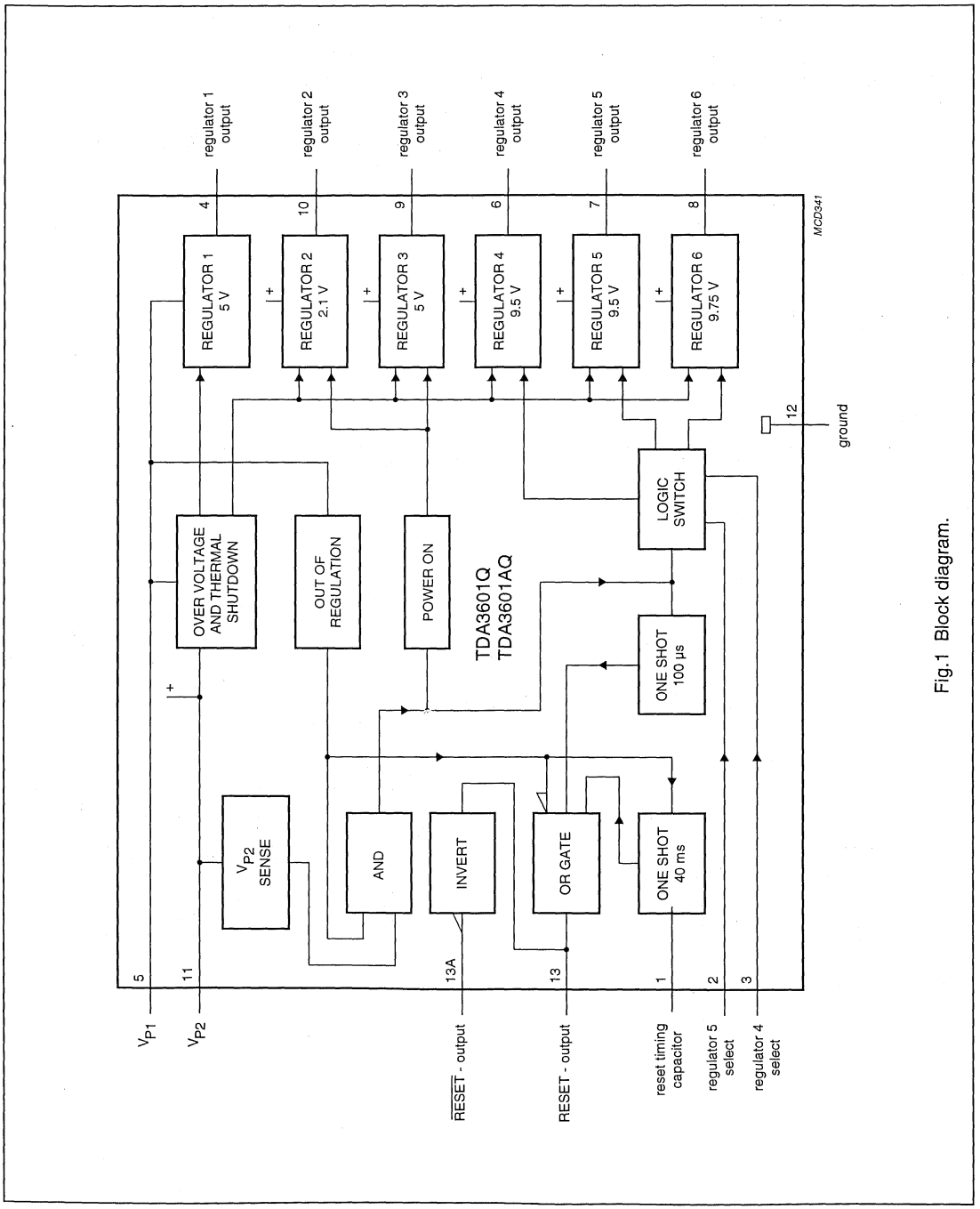


Fig.1 Block diagram.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3601Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6
TDA3601AQ			

GENERAL DESCRIPTION

The circuit contains five fixed voltage regulators with foldback current protection and one fixed voltage regulator (REGULATOR 1) that also operates during a load dump. In addition, a RESET function (TDA3601Q) or $\overline{\text{RESET}}$ function (TDA3601AQ), timer functions and a logic multiplexer are implemented.

PINNING

SYMBOL	PIN	DESCRIPTION
C_{RESET}	1	reset timing capacitor
R5-sel	2	regulator 5 select
R4-sel	3	regulator 4 select
REG1	4	regulator 1 output (5 V)
V_{P1}	5	supply voltage
REG4	6	regulator 4 output (9.5 V)
REG5	7	regulator 5 output (9.5 V)
REG6	8	regulator 6 output (9.75 V)
REG3	9	regulator 3 output (5 V)
REG2	10	regulator 2 output (2.4 V)
V_{P2}	11	supply voltage
GND	12	ground
RES	13	RESET output (TDA3601Q)
$\overline{\text{RES}}$	13A	$\overline{\text{RESET}}$ output (TDA3601AQ)

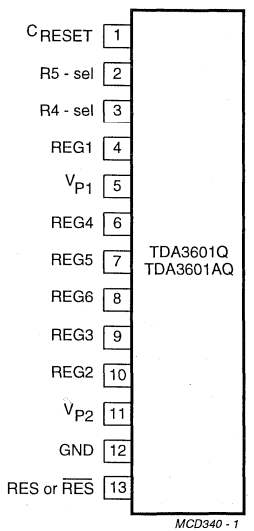


Fig.2 Pin configuration.

Multiple voltage regulator with switch TDA3603

FEATURES

- One V_P state controlled regulator (regulator 2)
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- One control pin for switching regulator 1 and the power switch
- Supply voltage range of −18 to +50 V (operating from 9.75 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1 is switched off, standby)
- Ignition input/output
- Reset output
- High ripple rejection
- Power switch.

PROTECTIONS

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be shortened)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1 and 2
- Delayed second current limit protection for the power switch
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3603 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller.

It contains one fixed voltage regulator with a foldback current protection (regulator 1) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.

There is a power switch with protections, operated by the enable input.

The reset and ignition outputs can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the ignition output indicates ignition voltage available.

The supply pin can withstand load dump pulses and negative supply voltages.

Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3603	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA3603P	HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	regulator 2 on	note 1	2.4	14.4	25	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	total quiescent current	standby mode	–	400	500	µA
T_{vj}	operating virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5\ mA \leq I_{REG1} \leq 300\ mA$	8.65	9.0	9.35	V
V_{REG2}	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 30\ mA$; $V_P = 14.4\ V$	4.8	5.0	5.2	V
$V_{drop(REG1)}$	drop-out voltage	$I_{REG1} = 0.3\ A$; note 2	–	–	0.5	V
Power switch						
$V_{drop(sw)}$	drop-out voltage	$I_{sw} = 0.3\ A$; note 3	–	–	0.9	V
I_M	peak current	$t \leq 10$ ms	1.4	–	–	A

Notes

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The drop-out voltage of regulator 1 is measured between V_P and V_{REG1}.
3. The drop-out voltage of the power switch is measured between V_P and V_{sw}.

BLOCK DIAGRAM

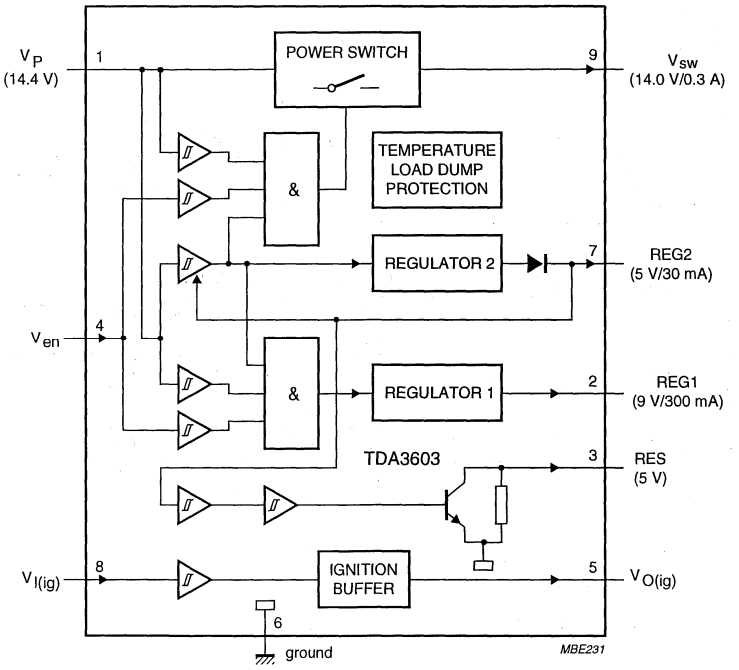


Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	SOT110-1	SOT398-1	
V_P	1	1	supply voltage
REG1	2	2	regulator 1 output
RES	3	3	reset output voltage (+5 V)
V_{en}	4	4	enable input voltage
$V_{O(ig)}$	5	5	ignition output voltage
GND	6	6	ground (0 V)
REG2	7	7	regulator 2 output
$V_{I(ig)}$	8	8	ignition input voltage
V_{sw}	9	9	power switch output voltage
i.c.	–	10 to 18	can be connected to a heat spreader

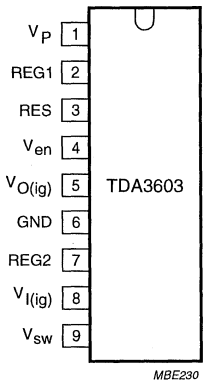
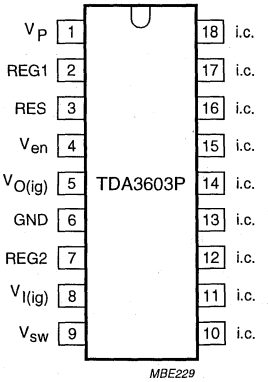


Fig.2 Pin configuration for SOT110-1.



Pins 10 to 18 can be connected to a heat spreader.

Fig.3 Pin configuration for SOT398-1.

Multiple voltage regulator with external reset delay and switch

TDA3604

FEATURES

- One V_P state controlled regulator (regulator 2)
- Regulator 2, reset and ignition buffer operates during load dump and thermal shutdown
- Separate control pins for switching regulator 1 and the power switch
- Supply voltage range of −18 to 50 V (operating from 9.75 V)
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1 is switched off, standby)
- Ignition input/output
- Reset output
- Reset delay time adjustable
- High ripple rejection
- Power switch
- Separate supply for the power switch.

PROTECTIONS

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be shortened)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1 and 2
- Delayed second current limit protection for the power-switch
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P.

GENERAL DESCRIPTION

The TDA3604 is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller.

It contains one fixed voltage regulator with a foldback current protection (regulator 1) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.

There is a power switch with protections, operated by an enable input.

The reset and ignition outputs can be used to interface by the microcontroller. The reset-signal can be used to call up the microcontroller and the ignition output indicates ignition voltage available.

Both supply pins can withstand load dump pulses and negative supply voltages.

Regulator 2 will be switched on at a supply voltage >6.5 V and off at a voltage of regulator 2 <1.9 V.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3604	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating		9.75	14.4	25	V
	regulator 2 on	note 1	2.4	14.4	25	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
I_q	total quiescent current	standby mode	–	400	500	µA
T_{vj}	operating virtual junction temperature		–	–	150	°C
Voltage regulators						
V_{REG1}	output voltage regulator 1	$0.5\ mA \leq I_{REG1} \leq 300\ mA$	8.65	9.0	9.35	V
V_{REG2}	output voltage regulator 2	$0.5\ mA \leq I_{REG2} \leq 30\ mA$; $V_P = 14.4\ V$	4.8	5.0	5.2	V
$V_{drop(REG1)}$	drop-out voltage	$I_{REG1} = 0.3\ A$; note 2	–	–	0.5	V
Power switch						
$V_{drop(sw)}$	drop-out voltage	$I_{sw} = 0.5\ A$; note 3	–	–	1.4	V
I_M	peak current	$t \leq 10$ ms	1.4	–	–	A

Notes

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The drop-out voltage of regulator 1 is measured between V_P and $V_{REG\ 1}$.
3. The drop-out voltage of the power switch is measured between V_P and V_{sw}.

BLOCK DIAGRAM

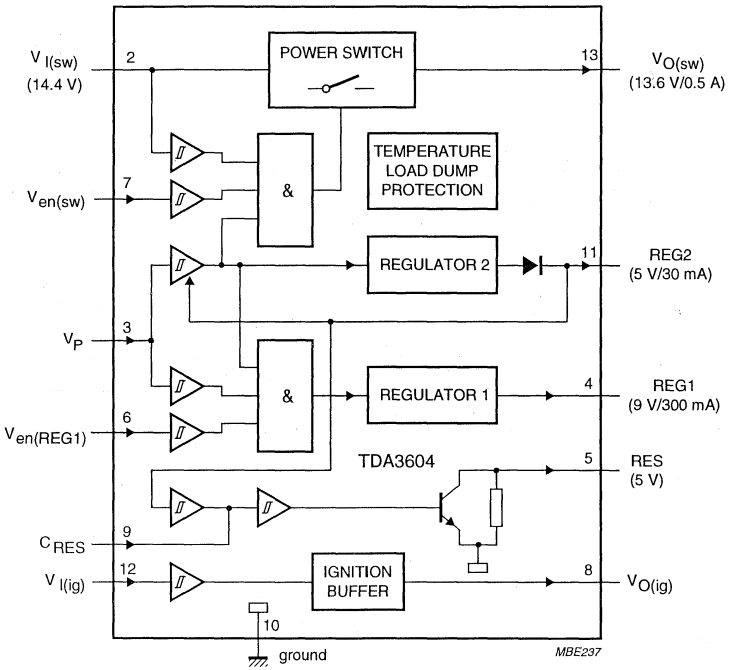


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
$V_{I(sw)}$	2	power switch input voltage
V_P	3	supply voltage
REG1	4	regulator 1 output
RES	5	reset output voltage (+5 V)
$V_{en(REG1)}$	6	regulator 1 enable input
$V_{en(sw)}$	7	power switch enable input voltage
$V_{O(ig)}$	8	ignition output voltage
C_{RES}	9	reset capacitor
GND	10	ground (0 V)
REG2	11	regulator 2 output
$V_{I(ig)}$	12	ignition input voltage
$V_{O(sw)}$	13	power switch output voltage

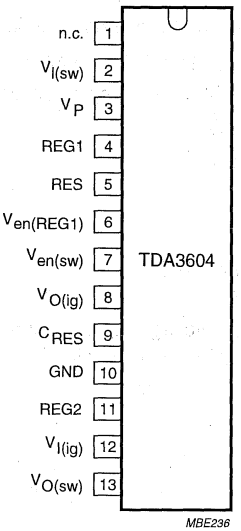


Fig.2 Pin configuration.

Multiple voltage regulator with battery detection

TDA3606

FEATURES

- One V_P-state controlled regulator
- Regulator and reset outputs operate during load dump
- Supply voltage range of −18 to +50 V
- Low quiescent current (battery detection switched off)
- High ripple rejection
- Dual reset output.

PROTECTIONS

- Reverse polarity safe (down to −18 V without high reverse current)
- Able to withstand voltages up to 18 V at the output (supply line may be short-circuited)
- ESD protected on all pins
- Load dump protection
- Foldback current limit protection for regulator
- DC short-circuit safe to ground and V_P of regulator output.

GENERAL DESCRIPTION

The TDA3606 is a low power voltage regulator. It contains:

1. One fixed voltage regulator with a foldback current protection, intended to supply a microcontroller, that also operates during load dump
2. A reset-signal can be used to interface with the microcontroller
3. Supply pin can withstand load dump pulses and negative supply voltages
4. Defined start-up behaviour; regulator will be switched on at a supply voltage higher than 7.6 V and off when the output voltage of the regulator drops below 2.4 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage					
	operating	regulator on	5.6	14.4	25	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(tot)}$	total quiescent supply current	standby mode	–	95	120	μA
Voltage regulator						
V_{REG}	output voltage regulator	$7\ V \leq V_P \leq 18\ V$	4.85	5.0	5.15	V
		$0.5\ mA \leq I_{REG} \leq 50\ mA$	4.8	5.0	5.2	V
V_{REGd}	drop-out voltage	$I_{REG} = 50\ mA$	–	–	0.4	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3606T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

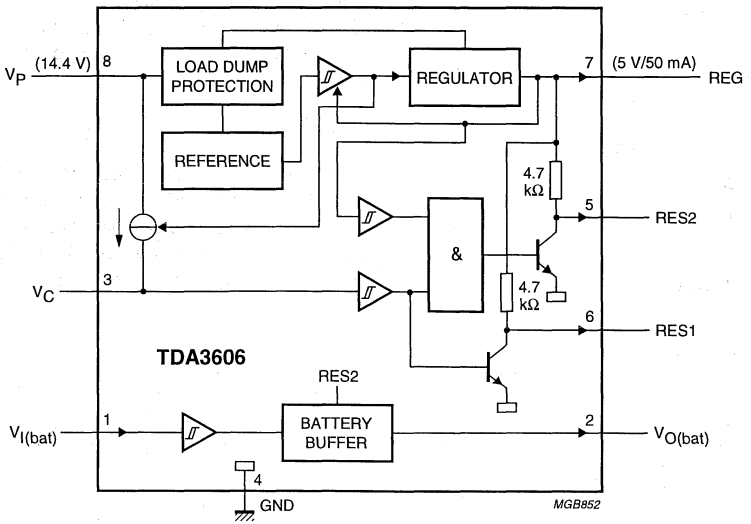


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{I(bat)}$	1	battery input voltage
$V_{O(bat)}$	2	battery output voltage
V_C	3	reset delay capacitor
GND	4	ground (0 V)
RES2	5	reset 2 output
RES1	6	reset 1 output
REG	7	regulator output
V_P	8	supply voltage

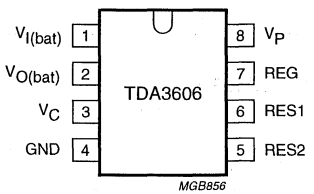


Fig.2 Pin configuration.

Stereo BTL audio output amplifier with DC volume control

TDA7053A

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2 × 1 W) and TDA7053AT (2 × 0.5 W) are stereo BTL output amplifiers with DC volume control. The devices are designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	–	W
	TDA7053AT	R_L = 16 Ω	0.5	0.6	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 6 V; R_L = ∞	–	22	25	mA
THD	total harmonic distortion					
	TDA7053A	P_{out} = 0.5 W	–	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7053A	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA7053AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

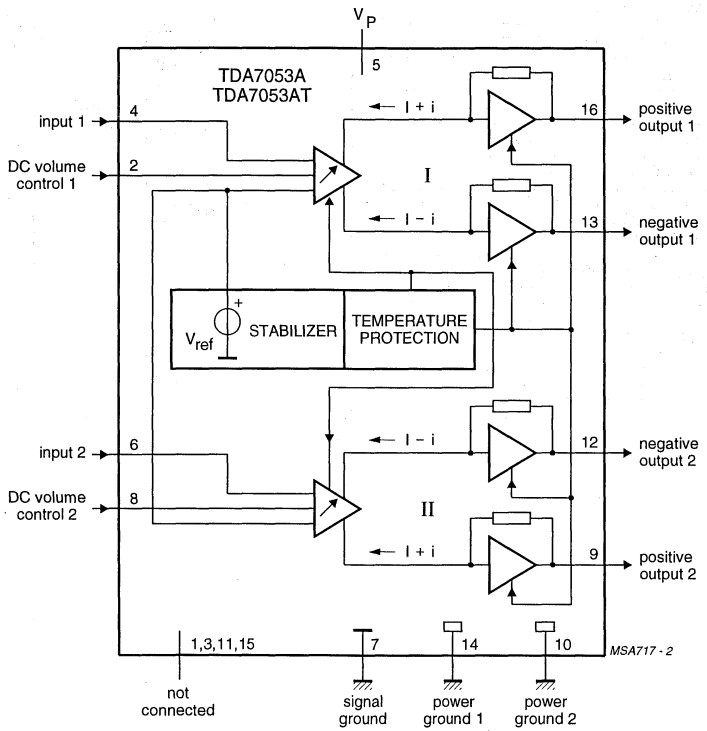


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume control 1
n.c.	3	not connected
$V_{I\,(1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I\,(2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume control 2
OUT2+	9	positive output 2
PGND2	10	power ground 2
n.c.	11	not connected
OUT2–	12	negative output 2
OUT1–	13	negative output 1
PGND1	14	power ground 1
n.c.	15	not connected
OUT1+	16	positive output 1

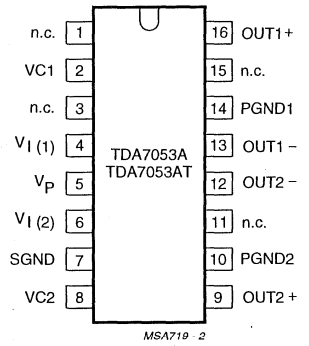


Fig.2 Pin configuration.

2 x 5 W stereo BTL audio output amplifier with DC volume control

TDA7057AQ

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is a stereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_P = 12 V; R_L = 16 Ω	3.0	3.5	–	W
		V_P = 12 V; R_L = 8 Ω	–	5.3	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_P = 12 V; R_L = ∞	–	22	25	mA
THD	total harmonic distortion	P_{out} = 0.5 W	–	0.3	1	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

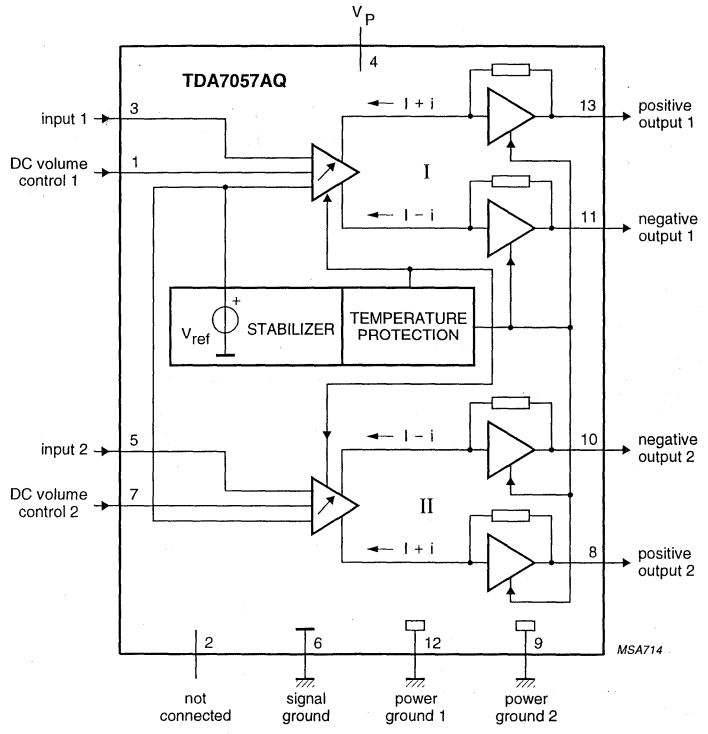


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume control 1
n.c.	2	not connected
$V_{I(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume control 2
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2–	10	negative output 2
OUT1–	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1

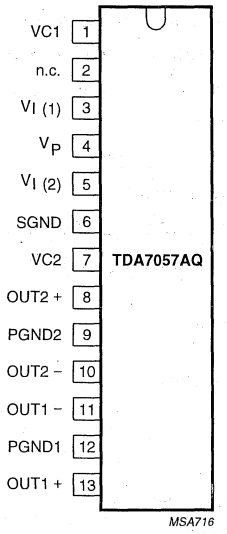


Fig.2 Pin configuration.

1 W BTL audio amplifier TDA8541

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8541(T) is a one channel audio power amplifier for an output power of 1 W with an 8 Ω load at a 5 V supply. The circuit contains a BTL amplifier with a complementary PNP-NPN output stage and standby/mute logic. The TDA8541T comes in an 8 pin SO package and the TDA8541 in an 8 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Telephony.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	8	12	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8541T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA8541	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1

BLOCK DIAGRAM

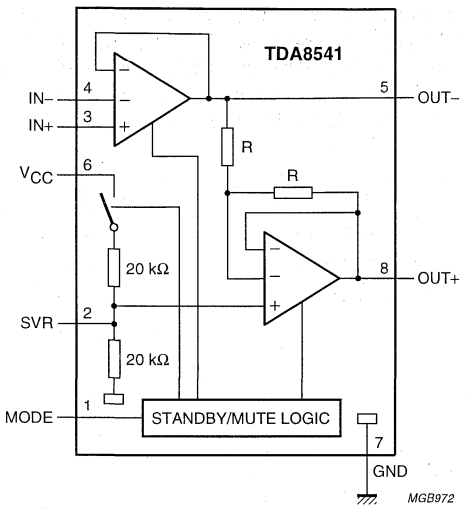


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
MODE	1	operating mode select (standby, mute, operating)
SVR	2	half supply voltage, decoupling ripple rejection
IN+	3	positive input
IN−	4	negative input
OUT−	5	negative loudspeaker terminal
V_{CC}	6	supply voltage
GND	7	ground
OUT+	8	positive loudspeaker terminal

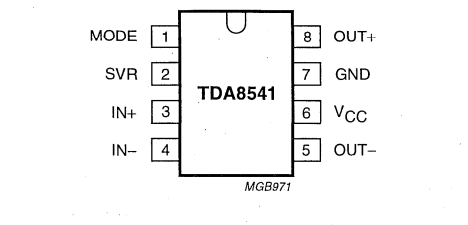


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8541(T) is a 1 W BTL audio power amplifier capable of delivering 1 W output power to an 8 Ω load at THD = 10% using a 5 V power supply. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage. The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of an NPN power transistor. The total voltage loss is <1 V and with a 5 V supply voltage and an 8 Ω loudspeaker an output power of 1 W can be delivered.

Mode select pin

The device is in standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} − 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1.5 V and V_{CC} − 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output, caused by charging of the input capacitor.

2 × 1 W BTL audio amplifier TDA8542

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8542(T) is a two channel audio power amplifier for an output power of 2 × 1 W with an 8 Ω load at a 5 V supply. The circuit contains two BTL amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The TDA8542T comes in a 16 pin SO package and the TDA8542 in a 16 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Motor-driver (servo).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	15	22	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 5 V	1	–	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8542T	SO16L	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8541	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

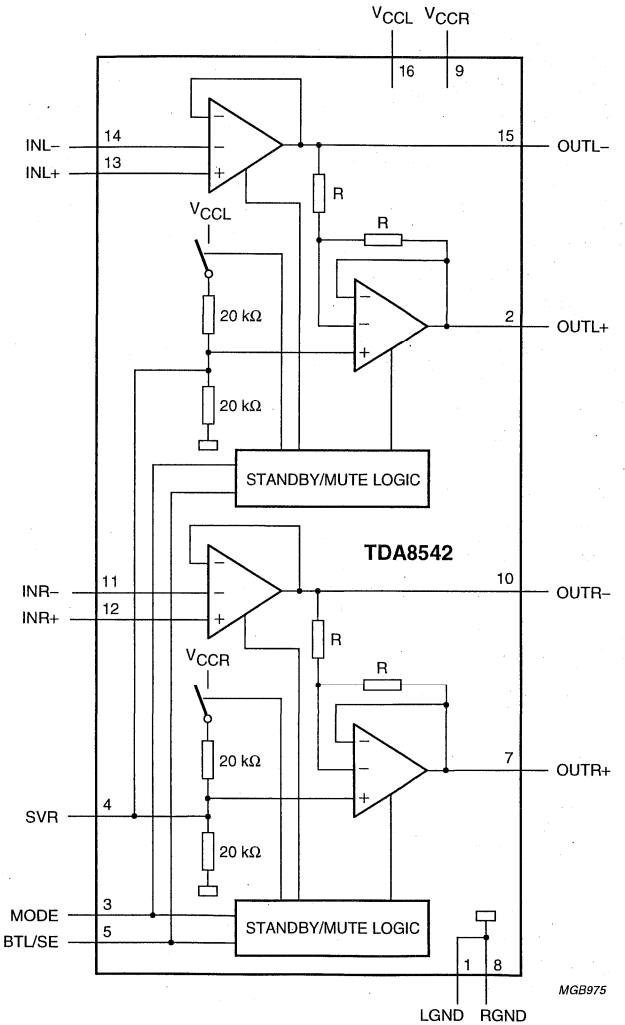


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LGND	1	ground, left channel
OUTL+	2	positive loudspeaker terminal, left channel
MODE	3	operating mode select (standby, mute, operating)
SVR	4	half supply voltage, decoupling ripple rejection
BTL/SE	5	BTL loudspeaker or SE headphone operation
n.c.	6	not connected
OUTR+	7	positive loudspeaker terminal, right channel
RGND	8	ground, right channel
V_{CCR}	9	supply voltage, right channel
OUTR–	10	negative loudspeaker terminal, right channel
INR–	11	negative input, right channel
INR+	12	positive input, right channel
INL+	13	positive input, left channel
INL–	14	negative input, left channel
OUTL–	15	negative loudspeaker terminal, left channel
V_{CCL}	16	supply voltage, left channel

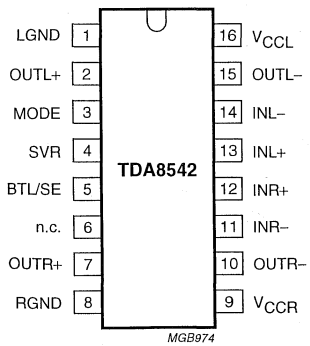


Fig.2 Pin configuration.

2 × 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8560Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8560Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package.
It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\lvert Z_I \rvert$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	45	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		39	40	41	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	250	μV
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	200	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8560Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

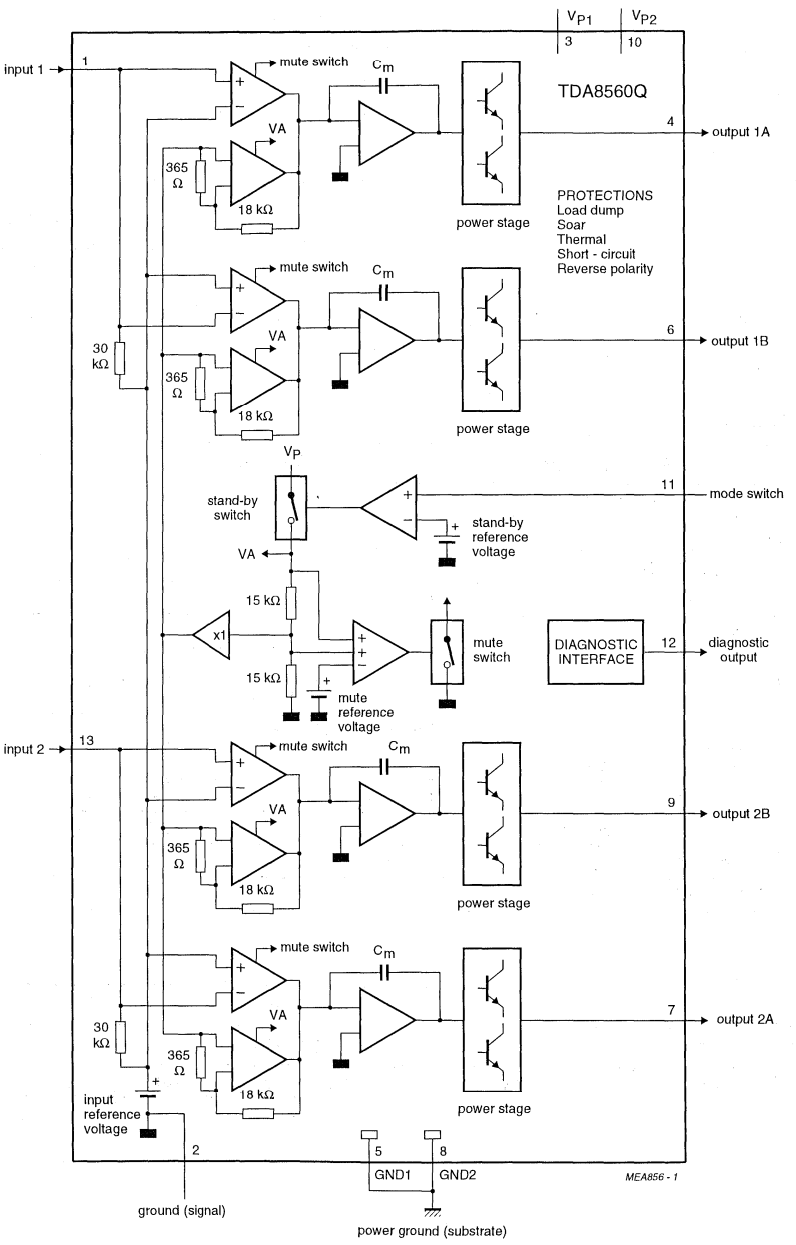


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

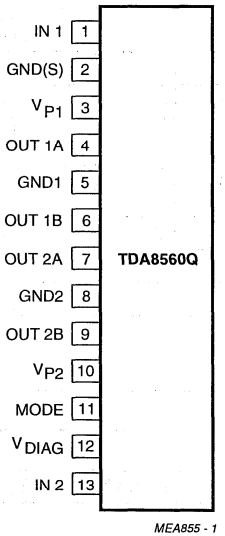


Fig.2 Pin configuration.

2 × 40 W/2 Ω stereo BTL car radio power amplifier with diagnostic facility

TDA8563Q

FEATURES

- Requires very few external components
- High output power
- 4 Ω and 2 Ω load impedance
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit safe to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8563Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package.
It contains 2 × 40 W/2 Ω amplifiers in BTL configuration.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\lvert Z_I \rvert$	input impedance		25	30	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	25	–	W
		R_L = 2 Ω; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	120	μV
$\lvert \Delta V_O \rvert$	DC output offset voltage		–	–	150	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8563Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

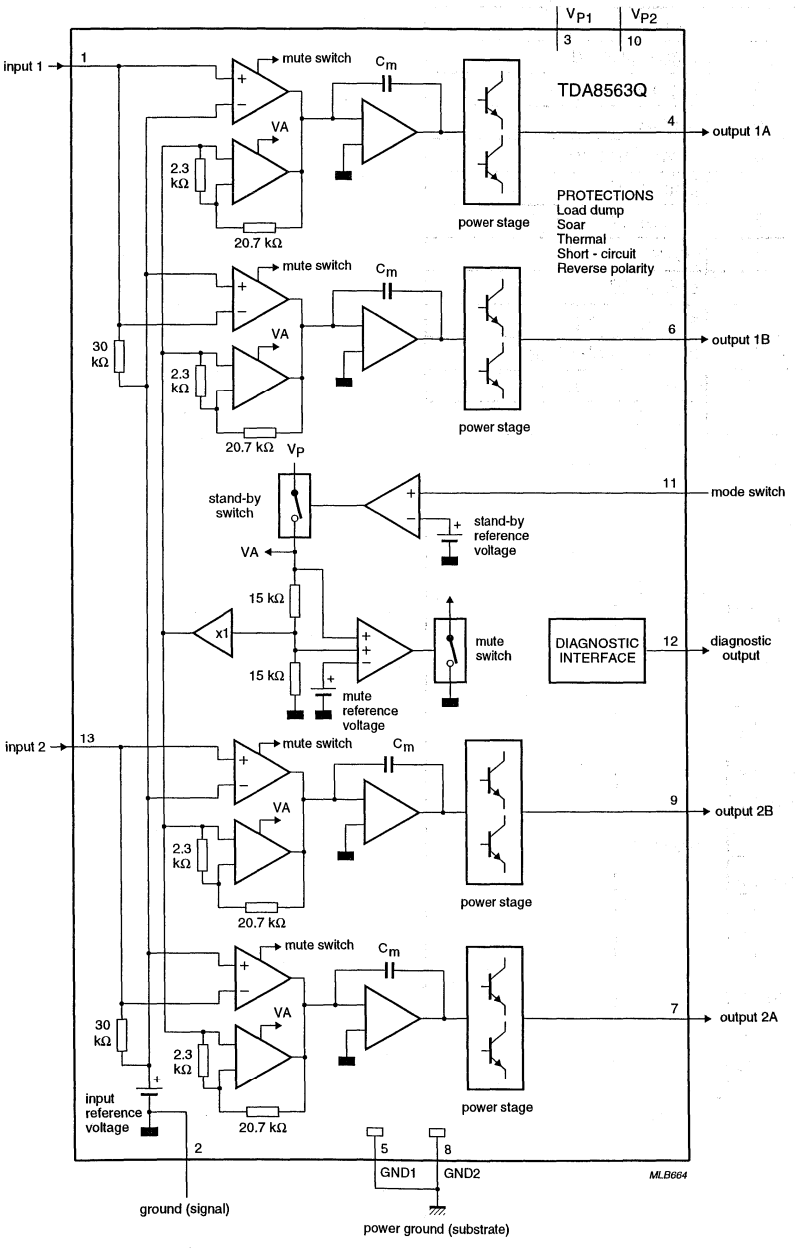


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage 1
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage 2
MODE	11	mode switch input
V_{DIAG}	12	diagnostic output
IN 2	13	input 2

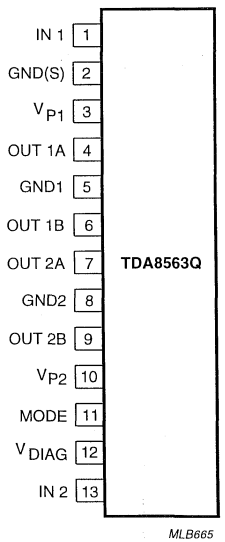


Fig.2 Pin configuration.

2 × 24 W BTL or 2 × 12 W single-ended car radio power amplifier

TDA8564Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use - Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8564Q is an integrated class-B output amplifier in a 17-lead DIL-bent-SIL power package. It contains 4 × 12 W single-ended or 2 × 24 W bridge amplifiers.

APPLICATIONS

- The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	80	–	mA
I_{stb}	standby current		–	0.1	100	μA
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10%	–	24	–	W
SVRR	supply voltage ripple rejection		–	41	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	200	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
Quad single-ended application						
P_o	output power	R_L = 4 Ω; THD = 10%	–	6.4	–	W
		R_L = 2 Ω; THD = 10%	–	12	–	W
SVRR	supply voltage ripple rejection		–	41	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	200	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8564Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

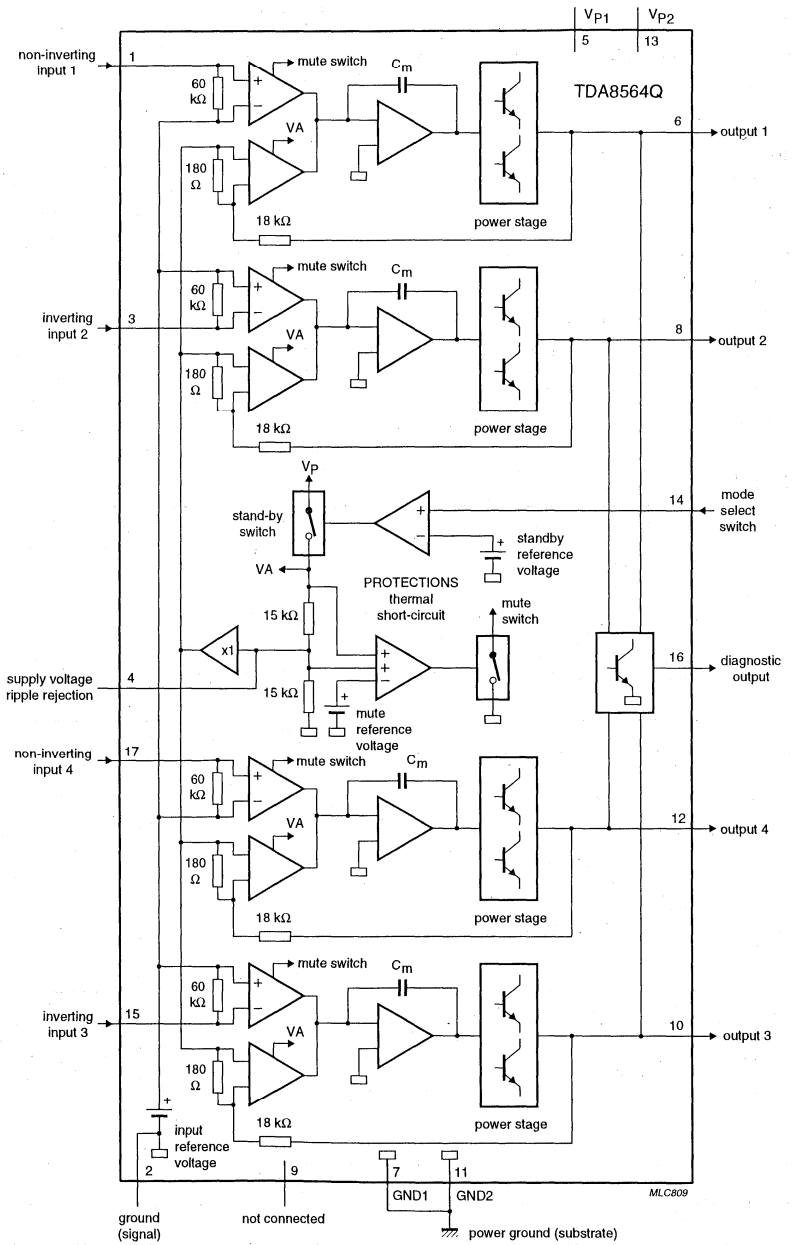


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
INV2	3	inverting input 2
SVRR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
n.c.	9	not connected
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{P2}	13	supply voltage 2
MODE	14	mode select switch input
INV3	15	inverting input 3
V_{DIAG}	16	diagnostic output
–INV4	17	non-inverting input 4

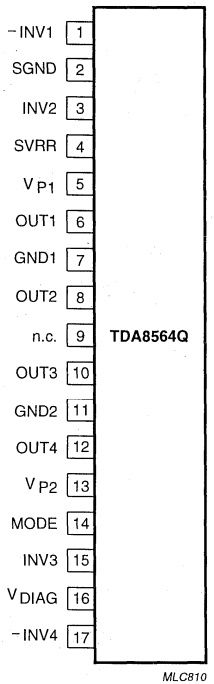


Fig.2 Pin configuration.

4 × 12 W single-ended car radio power amplifier with diagnostic interface

TDA8565Q

FEATURES

- Requires very few external components
- High output power
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs.

GENERAL DESCRIPTION

The TDA8565Q is an integrated class-B output amplifier in a 17-lead DIL-bent-to-SIL power package. It contains 4 × 12 W single-ended amplifiers.

APPLICATIONS

- The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	88	–	mA
I_{sb}	standby current		–	0.1	100	μA
$\lvert Z_I \rvert$	input impedance		50	–	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 10%	–	6.4	–	W
		R_L = 2 Ω; THD = 10%	–	12	–	W
SVRR	supply voltage ripple rejection		–	41	–	dB
V_{no}	noise output voltage	R_S = 0 Ω	–	200	–	μV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8565Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

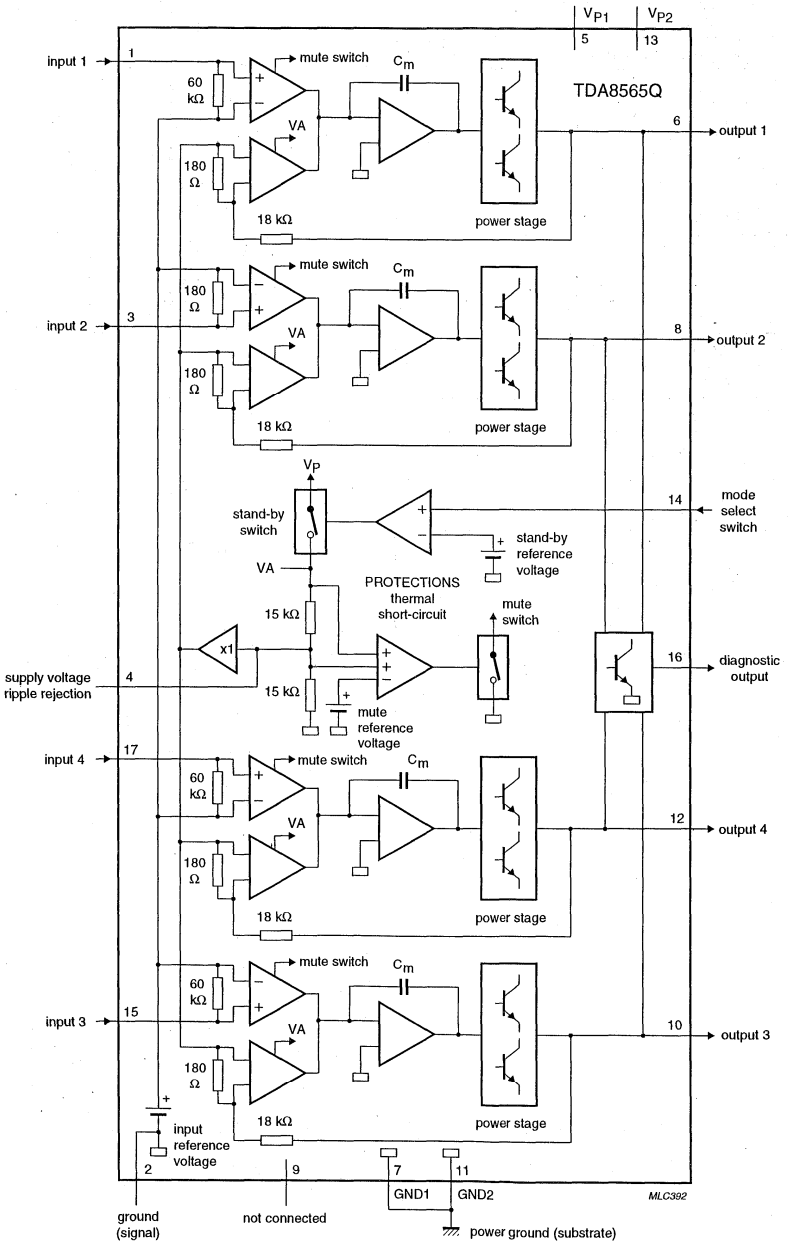


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1	1	input 1
SGND	2	signal ground
IN2	3	input 2
SVRR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
n.c.	9	not connected
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{P2}	13	supply voltage 2
MODE	14	mode select switch input
IN3	15	input 3
V_{DIAG}	16	diagnostic output
IN4	17	input 4

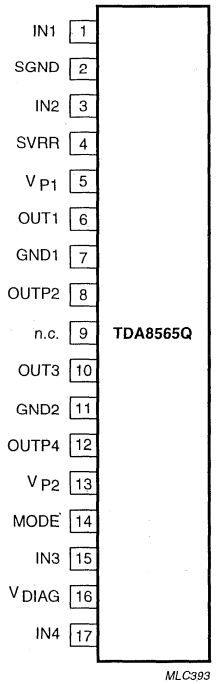


Fig.2 Pin configuration.

2 x 25 W BTL stereo car radio power amplifier with differential inputs and diagnostic outputs

TDA8566Q

FEATURES

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 Ω and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to V_P and across the load
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8566Q is an integrated class-B output amplifier contained in a 17-lead single-in-line (SIL; bent to DIL) plastic power package. The device contains two amplifiers in a Bridge-Tied Load configuration (BTL). The output power is 2 × 25 W in a 4 Ω load or 2 × 40 W in a 2 Ω load. It has a differential input stage and two diagnostic outputs. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{stb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
Z_i	input impedance		100	120	–	kΩ
P_{out}	output power	R_L = 4 Ω: THD = 10%	–	25	–	W
		R_L = 2 Ω: THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	R_s = 0 Ω	–	60	–	dB
α_{cs}	channel separation	R_s = 10 kΩ	–	50	–	dB
CMRR	common mode rejection ratio		–	75	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	–	120	μV
V_{os}	DC output offset voltage		–	–	100	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8566Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

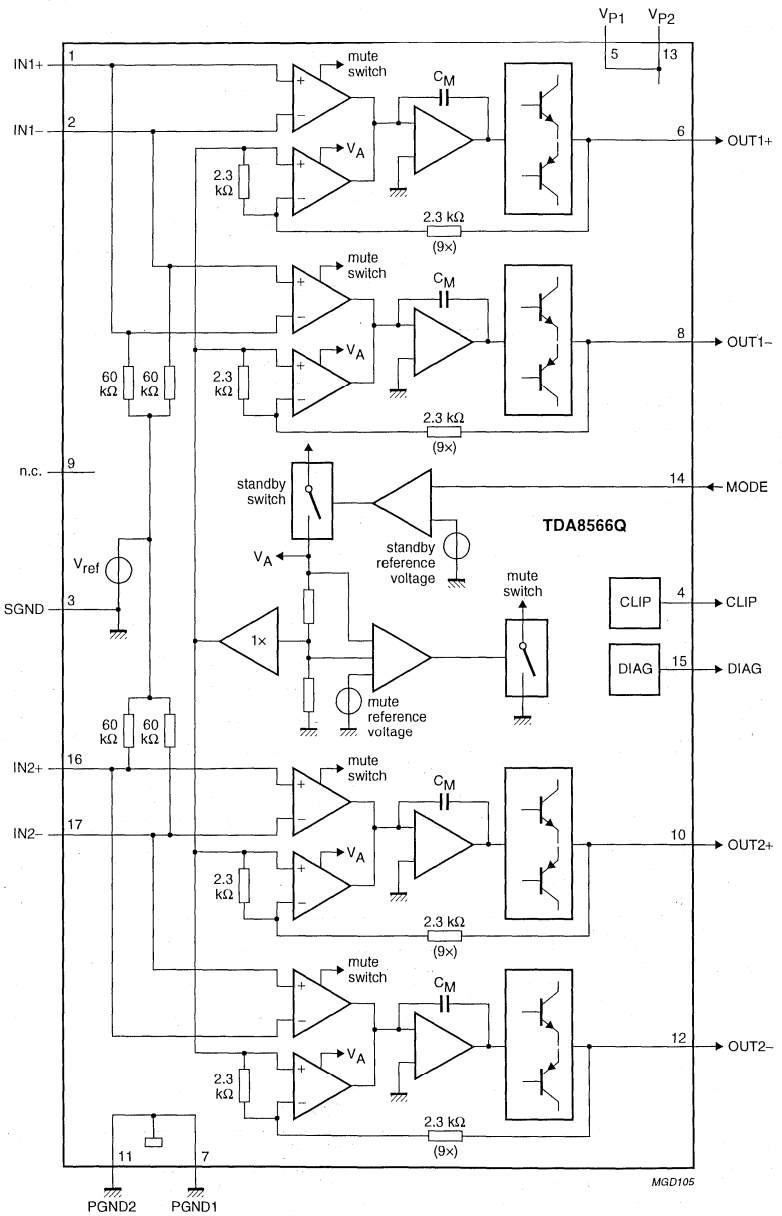


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IN1+	1	channel 1 input positive
IN1−	2	channel 1 input negative
SGND	3	small signal ground
CLIP	4	clip-detection
V_{P1}	5	supply voltage 1
OUT1+	6	channel 1 speaker output positive
PGND1	7	channel 1 negative power supply (ground)
OUT1−	8	channel 1 speaker output negative
n.c.	9	not connected
OUT2+	10	channel 2 speaker output positive
PGND2	11	channel 2 negative power supply (ground)
OUT2−	12	channel 2 speaker output negative
V_{P2}	13	supply voltage 2
MODE	14	mode select switch (stand-by/mute/operating)
DIAG	15	short-circuit and temperature pre-warning diagnostic
IN2+	16	channel 2 input positive
IN2−	17	channel 2 input negative

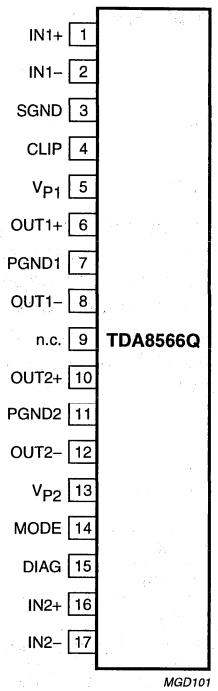


Fig.2 Pin configuration.

Class-H high-output voltage level line driver

TDA8574

FEATURES

- Output voltage swing larger than supply voltage
- High supply voltage ripple rejection
- Low distortion
- Low noise
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA8574(T) is a two channel class-H high-output voltage line driver for use in car audio applications. The line driver behaves as a non-inverting amplifier with a gain of 8 dB and a single-ended output. Due to the class-H voltage lifting principle the voltage swing over the load is more than the supply voltage. With a supply voltage of 9 V the output voltage swing over the load will be 14 V (peak-to-peak).

The TDA8574 is available in a DIP16 package and the TDA8574T in a SO16 package. Line drivers are necessary in car audio systems in which the power amplifiers are driven by long cables. The signal-to-noise ratio of these car audio systems is improved by using the TDA8574(T) class-H high-output level line driver. The high-output level of TDA8574(T) enables a reduction of the gain of the power amplifier resulting in an improvement in power amplifier performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		6	9	12	V
I_{CC}	supply current	V_{CC} = 9 V	–	9	13	mA
G_v	voltage gain		7.5	8	8.5	dB
$V_{o(rms)}$	maximal output voltage (RMS value)	THD = 0.1%	5.0	–	–	V
SVRR	supply voltage ripple rejection		50	65	–	dB
THD	total harmonic distortion	$V_{o(rms)}$ = 3 V; f = 1 kHz	–	0.003	–	%
V_{no}	noise output voltage		–	5	–	μV
$\|Z_o\|$	dynamic output impedance		–	–	10	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8574T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8574	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4

BLOCK DIAGRAM

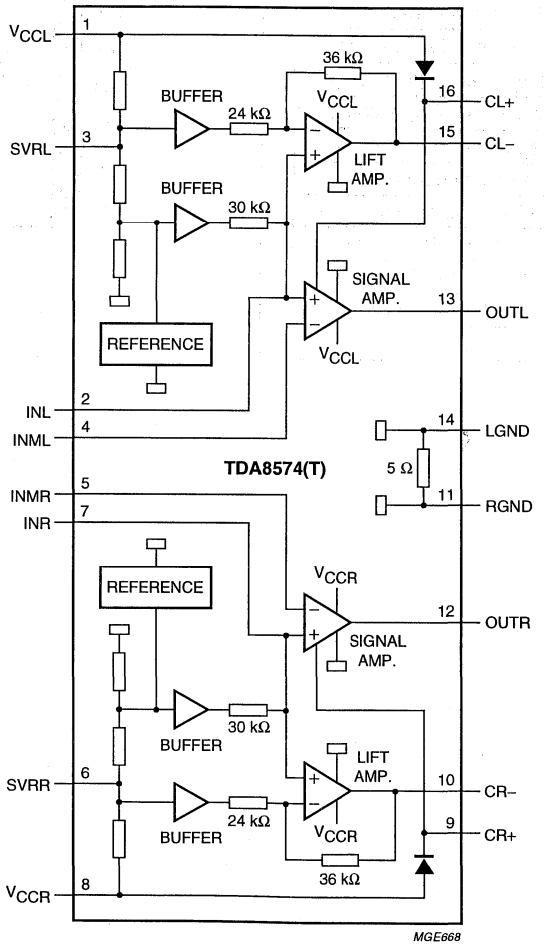


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCL}	1	supply voltage left channel
INL	2	input voltage left channel
SVRL	3	SVRR left channel
INML	4	inverting input left channel
INMR	5	inverting input right channel
SVRR	6	SVRR right channel
INR	7	input voltage right channel
V_{CCR}	8	supply voltage right channel
CR+	9	lift capacitor (+) right channel
CR–	10	lift capacitor (–) right channel
RGND	11	ground right channel
OUTR	12	output voltage right channel
OUTL	13	output voltage left channel
LGND	14	ground left channel
CL–	15	lift capacitor (–) left channel
CL+	16	lift capacitor (+) left channel

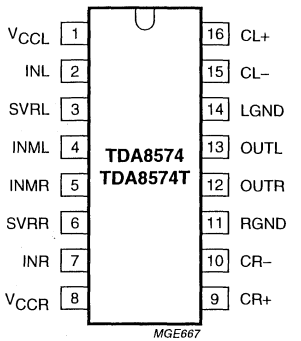


Fig.2 Pin configuration.

Class-H high-output voltage level line driver

TDA8576T

FEATURES

- Output voltage swing larger than supply voltage
- High supply voltage ripple rejection
- Low distortion
- Low noise
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA8576T is a two channel class-H high-output voltage line driver for use in car audio applications. The line driver operates as a non-inverting amplifier with a gain of 6 dB and a single-ended output. Due to the class-H voltage lifting principle the voltage swing over the load is more than the supply voltage.

With a supply voltage of 9 V the output voltage swing over the load will be more than 14 V (peak-to-peak). The TDA8576T is available in a SO16 package.

Line drivers are necessary in car audio systems in which the power amplifiers are driven by long cables. The signal-to-noise ratio of these car audio systems is improved by using the TDA8576T class-H high-output level line driver. The high-output level of TDA8576T enables a reduction of the gain of the power amplifier resulting in an improvement of the power amplifier performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage range		6	9	12	V
I_{CC}	supply current	V_{CC} = 9 V	–	14	20	mA
G_v	voltage gain		–	6	–	dB
$V_{o(rms)}$	maximum output voltage (RMS value)	THD = 0.1%	5.0	–	–	V
SVRR	supply voltage ripple rejection		40	65	–	dB
THD	total harmonic distortion	$V_{o(rms)}$ = 3 V; f = 1 kHz	–	0.005	–	%
V_{no}	noise output voltage		–	5	–	μV
$\|Z_o\|$	dynamic output impedance		–	–	10	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8576T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

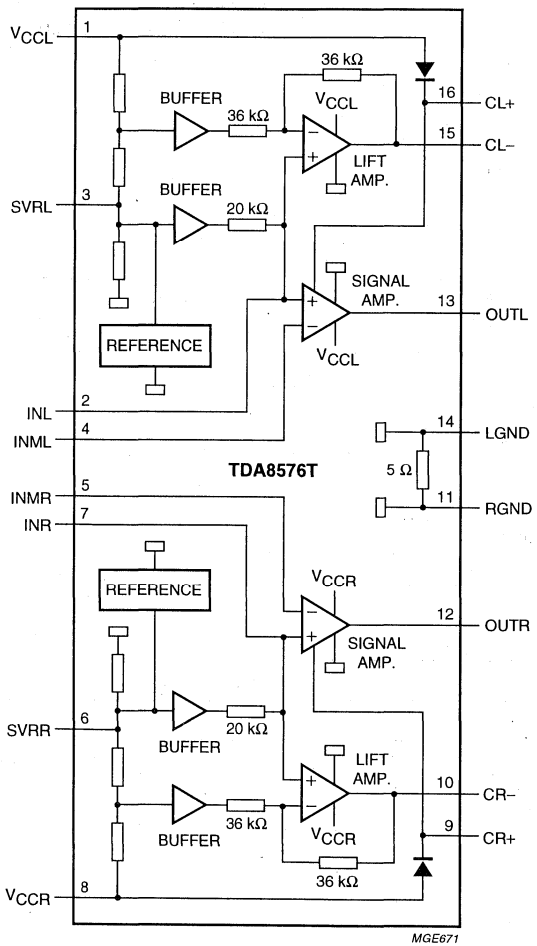


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCL}	1	supply voltage left channel
INL	2	input voltage left channel
SVRL	3	SVRR left channel
INML	4	inverting input left channel
INMR	5	inverting input right channel
SVRR	6	SVRR right channel
INR	7	input voltage right channel
V_{CCR}	8	supply voltage right channel
CR+	9	lift capacitor (+) right channel
CR–	10	lift capacitor (–) right channel
RGND	11	ground right channel
OUTR	12	output voltage right channel
OUTL	13	output voltage left channel
LGND	14	ground left channel
CL–	15	lift capacitor (–) left channel
CL+	16	lift capacitor (+) left channel

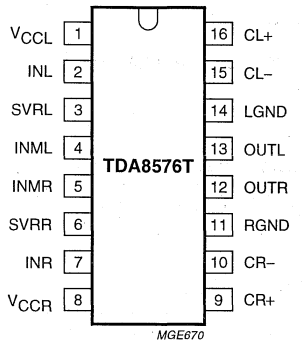


Fig.2 Pin configuration.

Dual common-mode rejection differential line receiver

TDA8577

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8577 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in a 9-pin single in-line package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8577	9	SIL9	plastic	SOT142

Dual common-mode rejection differential line receiver

TDA8577

BLOCK DIAGRAM

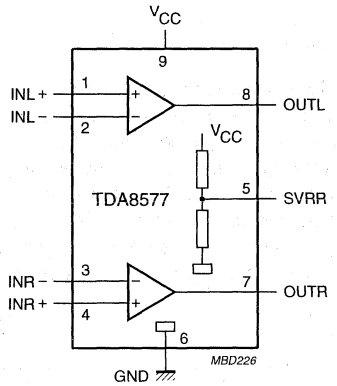


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8577 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8577 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
INL−	2	negative input left
INR−	3	negative input right
INR+	4	positive input right
SVRR	5	half supply voltage
GND	6	ground
OUTR	7	output right
OUTL	8	output left
V_{CC}	9	supply voltage

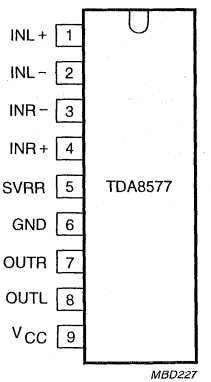


Fig.2 Pin configuration.

Dual common-mode rejection differential line receiver

TDA8578

FEATURES

- Excellent common-mode rejection up to high frequencies
- Elimination of source resistance in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- Protected against electrostatic discharge
- AC and DC short circuit safe to ground and V_{CC}
- Fast DC settling.

APPLICATIONS

- Audio
- Car radio.

GENERAL DESCRIPTION

The TDA8578 is a two-channel differential amplifier in a 16 pin DIL or SO package intended to receive line inputs in audio applications requiring a high-level of common-mode rejection. The amplifier has a gain of 0 dB and a low distortion. The device is primarily developed for those car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and ground noise has to be eliminated.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		–55	–60	–	dB
V_{no}	noise output voltage		–	3.7	5	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8578	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8578T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

Dual common-mode rejection differential line receiver

TDA8578

BLOCK DIAGRAM

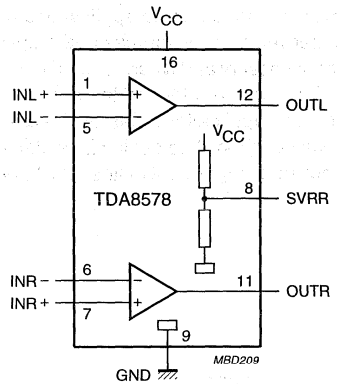


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8578 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals. The device has a very high-level of common-mode rejection and it eliminates ground noise. The common-mode rejection keeps constant up to high frequencies. The gain of the amplifiers is fixed at 0 dB. The inputs have a high-input impedance and the output stage is a class AB stage with a low-output impedance. For a large common-mode rejection also at low frequencies, an electrolytic input capacitor at the negative input pin is advised. The input impedance is relative high, this would result in a large settling time of the DC input voltage. Therefore a quick charge circuit is included that charges the input capacitor within 0.2 s.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
n.c.	2	not connected
n.c.	3	not connected
n.c.	4	not connected
INL−	5	negative input left
INR−	6	negative input right
INR+	7	positive input right
SVRR	8	half supply voltage
GND	9	ground
n.c.	10	not connected
OUTR	11	output right
OUTL	12	output left
n.c.	13	not connected
n.c.	14	not connected
n.c.	15	not connected
V_{CC}	16	supply voltage

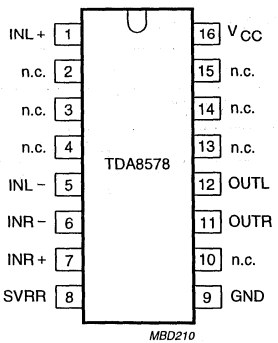


Fig.2 Pin configuration.

Dual common-mode rejection differential line receiver

TDA8579

FEATURES

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling.

GENERAL DESCRIPTION

The TDA8579 is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 8-pin small outline (SO) or dual in-line (DIP) package.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	11	14	mA
G_v	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	–	dB
V_{no}	noise output voltage		–	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	–	kΩ
CMRR	common-mode rejection ratio	R_s = 0 Ω	–	80	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8579	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA8579T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

Dual common-mode rejection differential line receiver

TDA8579

BLOCK DIAGRAM

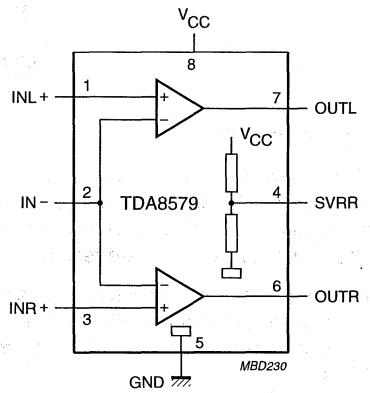


Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8579 contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8579 has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

PINNING

SYMBOL	PIN	DESCRIPTION
INL+	1	positive input left
IN−	2	common negative input
INR+	3	positive input right
SVRR	4	half supply voltage
GND	5	ground
OUTR	6	output right
OUTL	7	output left
V_{CC}	8	supply voltage

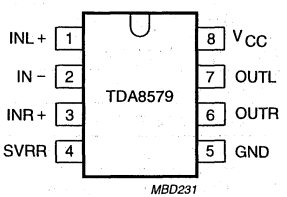


Fig.2 Pin configuration.

PLL frequency synthesizer TDA8735

FEATURES

- Complete 30 MHz single-chip tuning system
- Loop amplifier included
- 2-level current amplifier (charge pump) for adjusting the loop gain
- A powerful digital memory phase detector
- Programmable reference frequencies of 1 kHz, 10 kHz or 25 kHz
- I²C-bus interface
- Programmable address select input
- Software controlled switch output.

APPLICATIONS

- Satellite sound receiver
- Radio receiver: LW, MW and SW.

GENERAL DESCRIPTION

The TDA8735 is a single-chip PLL synthesizer designed for satellite receivers. The device can be set to two different addresses which can be used in applications where independently tuned VCOs are required.

To adapt to different frequency accuracy, 3 reference frequencies are selectable via the I²C-bus. The charge pump current can be set to 2 values with a ratio of 1 : 100 via the I²C-bus.

A programmable switch (open collector) is integrated to enable mode or normal switching, or other types of application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1}	8.5	12	V
I_{CC1}	supply current (pin 3)	outputs unloaded	12	20	28	mA
I_{CC2}	supply current (pin 16)	outputs unloaded	0.2	0.5	1	mA
$f_{i(max)}$	maximum input frequency		30	–	–	MHz
$f_{i(min)}$	minimum input frequency		–	–	512	kHz
$V_{i(rms)}$	input voltage (RMS value)		30	–	500	mV
P_{tot}	total power dissipation		–	0.14	–	W
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8735	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
TDA8735T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

BLOCK DIAGRAM

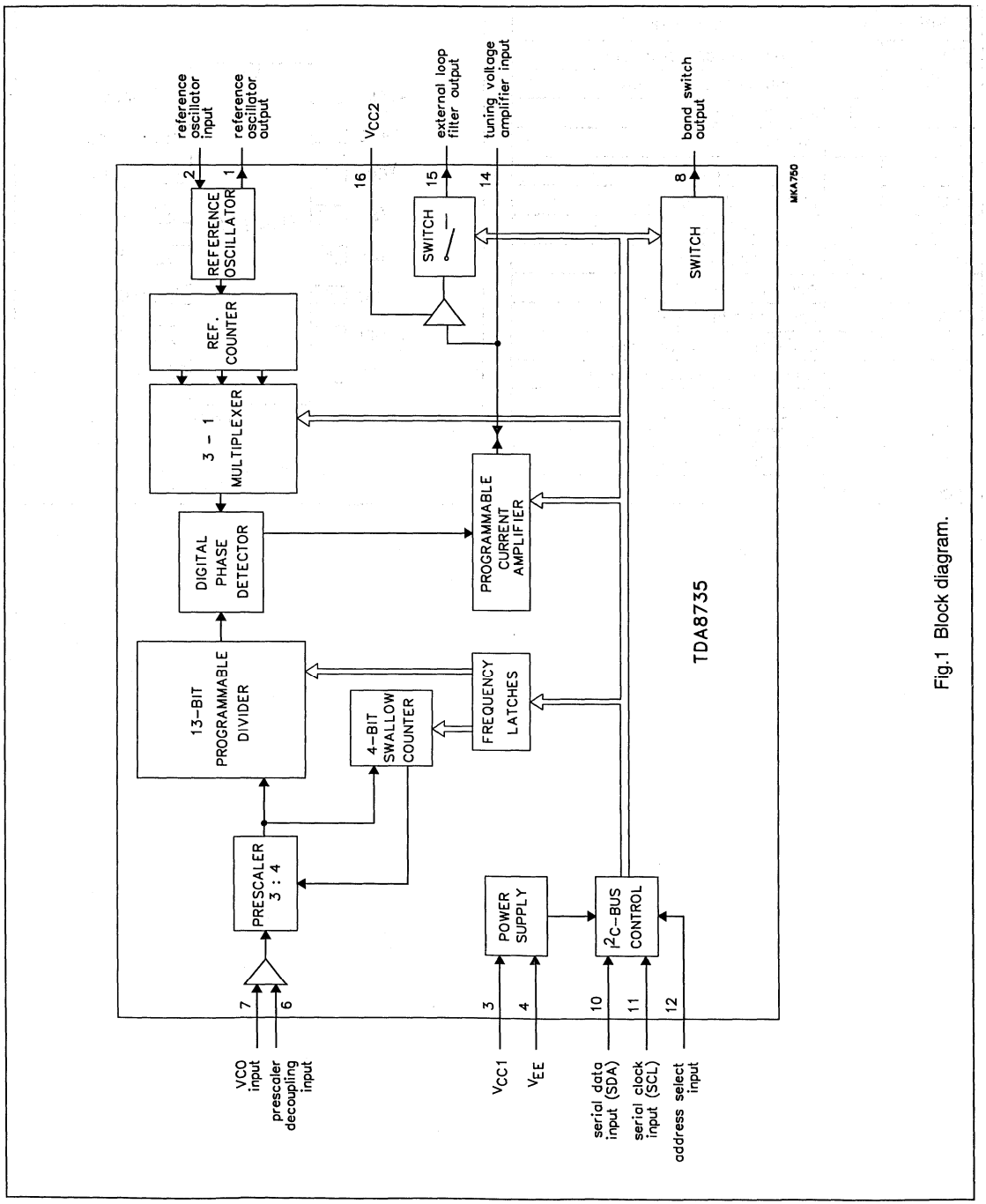


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XTAL1	1	reference oscillator output
XTAL2	2	reference oscillator input
V_{CC1}	3	supply voltage 1
V_{EE}	4	ground
n.c.	5	not connected
DEC	6	prescaler decoupling
VCOFI	7	VCO input frequency
BS	8	band switch output
n.c.	9	not connected
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
n.c.	13	not connected
$LOOP_I$	14	tuning voltage amplifier input
$LOOP_O$	15	external loop filter output
V_{CC2}	16	supply voltage 2

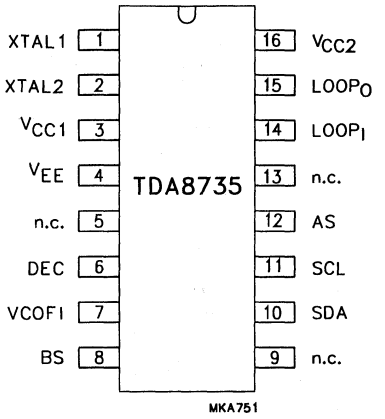


Fig.2 Pin configuration.

AM/FM stereo radio circuit TEA5711; TEA5711T

FEATURES

- Wide supply voltage range: 1.8 or 2.1 to 12 V
- Low current consumption: 15 mA at AM, 16 mA at FM
- High selectivity with distributed IF gain
- LED driver for stereo indication
- High input sensitivity: 1.6 mV/m (AM), 2.0 μV (FM) for 26 dB S/N
- Good strong signal behaviour: 10 V/m at AM, 500 mV at FM
- Low output distortion: 0.8% at AM, 0.3% at FM
- Signal level output
- Soft mute
- Signal dependent stereo
- Designed for simple and reliable printed-circuit board layout
- High impedance MOSFET input on AM.

APPLICATIONS

- Portable AM/FM stereo radio
- Mini/midi receiver sets
- Personal headphone radio.

DESCRIPTION

The TEA5711 is a high performance Bimos IC for use in AM/FM stereo radios. All necessary functions are integrated: from AM and FM front-end to AM detector and FM stereo output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	TYP.
V_P	dynamic supply voltage		1.8	–	12	V
V_P	static supply voltage		2.1	–	12	V
I_P	supply current					
	AM mode		11.9	15.0	18.9	mA
	FM mode		13.5	16.5	20.2	mA
T_{amb}	operating ambient temperature		−15	–	+60	°C
AM performance						
V_{in1}	RF sensitivity		40	55	70	μV
V_{28}	AF output voltage		36	45	70	mV
THD	total harmonic distortion		–	0.8	2.0	%
FM performance						
V_{in3}	RF sensitivity		1.0	2.0	3.8	μV
V_{28}	AF output voltage		50	61	72	mV
THD	total harmonic distortion		–	0.3	0.8	%
MPX performance						
α_{cs}	channel separation		26	30	–	dB
A_{MPX}	MPX voltage gain	V_{AF-L}/V_{in9}; S5 in position MONO	−1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5711	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA5711T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

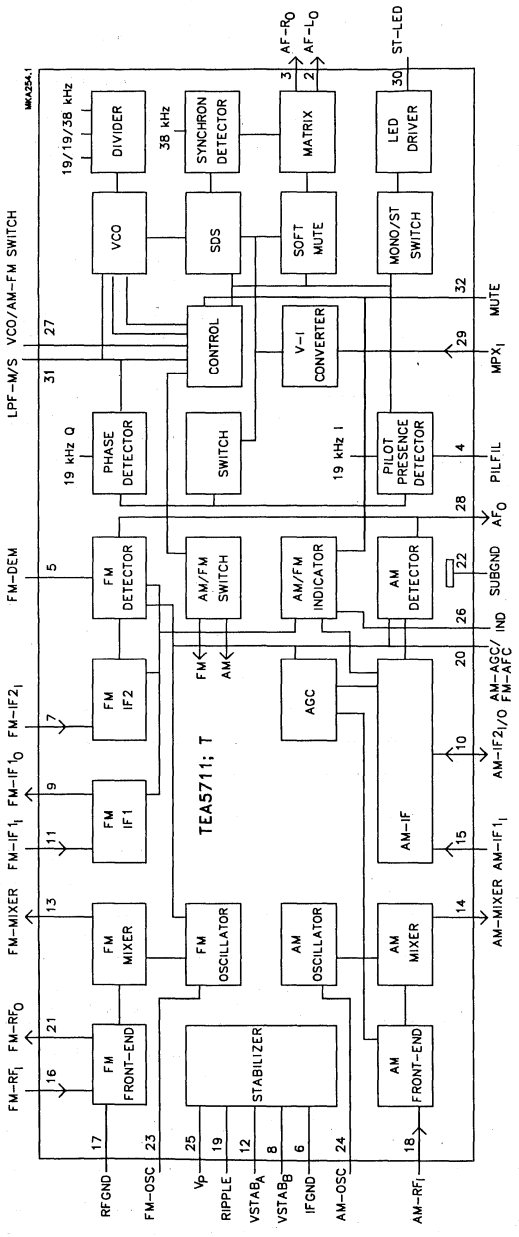


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
AF-L_O	2	left channel audio output (output impedance typ. 4.3 kΩ)
AF-R_O	3	right channel audio output (output impedance typ. 4.3 kΩ)
PILFIL	4	pilot detector filter pin
FM-DEM	5	ceramic discriminator pin
IFGND	6	ground of IF, detector and MPX stages
FM-$IF2_I$	7	second FM-IF input (input impedance typ. 330 Ω)
$VSTAB_B$	8	stabilized internal supply voltage (B)
FM-$IF1_O$	9	first FM-IF output (output impedance typ. 330 Ω)
AM-$IF2_{I/O}$	10	input/output to IFT; output: current source
FM-$IF1_I$	11	first FM-IF input (input impedance typ. 330 Ω)
$VSTAB_A$	12	stabilized internal supply voltage (A)
FM-MIXER	13	output to ceramic IF filter (output impedance typ. 330 Ω)
AM-MIXER	14	open-collector output to IFT
AM-$IF1_I$	15	input from IFT or ceramic filter (input impedance typ. 3 kΩ)
FM-RF_I	16	FM-RF aerial input (input impedance typ. 50 Ω)
RFGND	17	FM-RF ground
AM-RF_I	18	parallel tuned AM aerial circuit to ground (total input capacitance typ. 3 pF)
RIPPLE	19	ripple capacitor pin
AM-AGC/FM-AFC	20	AGC/AFC capacitor pin
FM-RF_O	21	parallel tuned FM-RF circuit to ground
SUBGND	22	substrate and RF ground
FM-OSC	23	parallel tuned FM-oscillator circuit to ground
AM-OSC	24	parallel tuned AM-oscillator circuit to ground
V_P	25	positive supply voltage
IND	26	signal level output
VCO/AM-FM SWITCH	27	VCO and switch terminal: open for AM; ground for FM
AF_O	28	AM/FM AF output (output impedance typ. 5 kΩ)
MPX_I	29	input for stereo decoder (input impedance typ. 180 kΩ)
ST-LED	30	stereo indicator
LPF-M/S	31	pin for loop-filter and mono/stereo switch
MUTE	32	mute pin

AM/FM stereo DTS radio circuit TEA5712; TEA5712T

FEATURES

- Wide supply voltage range: 1.8 or 2.1 to 12 V
- Low current consumption: 16 mA at AM, 17 mA at FM
- High selectivity with distributed IF gain
- LED driver for stereo indication
- High input sensitivity: 1.6 mV/m (AM), 2.0 μV (FM) for 26 dB S/N
- Good strong signal behaviour: 10 V/m at AM, 500 mV at FM
- Low output distortion: 0.8% at AM, 0.3% at FM
- Signal level output
- Soft mute
- Signal dependent stereo
- IF output signals available for IF counting
- Designed for simple and reliable printed-circuit board layout
- High impedance MOSFET input on AM.

APPLICATIONS

- Portable AM/FM stereo radio
- Mini/midi receiver sets
- Digitally tuned personal headphone radio.

DESCRIPTION

The TEA5712 is a high performance Bimos IC for use in digitally tuned AM/FM stereo radios. All necessary functions are integrated: from AM and FM front-end to AM detector and FM stereo output stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	TYP.
V_P	dynamic supply voltage		1.8	–	12	V
V_P	static supply voltage		2.1	–	12	V
I_P	supply current					
	AM mode		12.8	16.0	20.0	mA
	FM mode		14.3	17.5	21.4	mA
T_{amb}	operating ambient temperature		−15	–	+60	°C
AM performance						
V_{in1}	RF sensitivity		40	55	70	μV
V_{28}	AF output voltage		36	45	70	mV
THD	total harmonic distortion		–	0.8	2.0	%
FM performance						
V_{in3}	RF sensitivity		1.0	2.0	3.8	μV
V_{28}	AF output voltage		50	61	72	mV
THD	total harmonic distortion		–	0.3	0.8	%
MPX performance						
α_{cs}	channel separation		26	30	–	dB
A_{MPX}	MPX voltage gain	V_{AF-L}/V_{in9}; S5 in position MONO	−1.5	0	+1.0	dB
THD	total harmonic distortion		–	0.5	1.0	%

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5712	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA5712T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

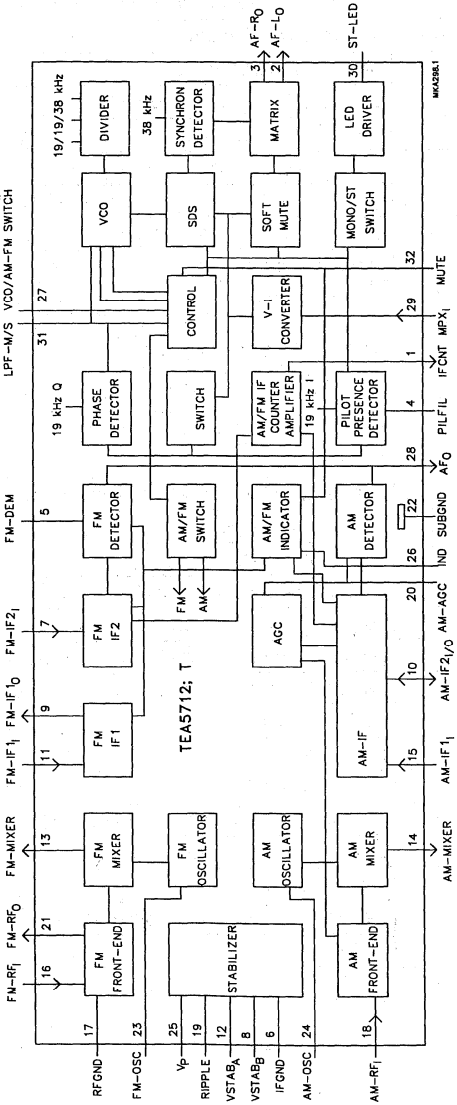


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
IFCNT	1	IF signal output for IF counting
AF-L_O	2	left channel audio output (output impedance typ. 4.3 kΩ)
AF-R_O	3	right channel audio output (output impedance typ. 4.3 kΩ)
PILFIL	4	pilot detector filter pin
FM-DEM	5	ceramic discriminator pin
IFGND	6	ground of IF, detector and MPX stages
FM-IF2_I	7	second FM-IF input (input impedance typ. 330 Ω)
$VSTAB_B$	8	stabilized internal supply voltage (B)
FM-IF1_O	9	first FM-IF output (output impedance typ. 330 Ω)
AM-IF$2_{I/O}$	10	input/output to IFT; output: current source
FM-IF1_I	11	first FM-IF input (input impedance typ. 330 Ω)
$VSTAB_A$	12	stabilized internal supply voltage (A)
FM-MIXER	13	output to ceramic IF filter (output impedance typ. 330 Ω)
AM-MIXER	14	open-collector output to IFT
AM-IF1_I	15	input from IFT or ceramic filter (input impedance typ. 3 kΩ)
FM-RF_I	16	FM-RF aerial input (input impedance typ. 50 Ω)
RFGND	17	FM-RF ground
AM-RF_I	18	parallel tuned AM aerial circuit to ground (total input capacitance typ. 3 pF)
RIPPLE	19	ripple capacitor pin
AM-AGC	20	AGC capacitor pin
FM-RF_O	21	parallel tuned FM-RF circuit to ground
SUBGND	22	substrate and RF ground
FM-OSC	23	parallel tuned FM-oscillator circuit to ground
AM-OSC	24	parallel tuned AM-oscillator circuit to ground
V_P	25	positive supply voltage
IND	26	stop signal output
VCO/AM-FM SWITCH	27	VCO and switch terminal: open for AM; ground for FM
AF_O	28	AM/FM AF output (output impedance typ. 5 kΩ)
MPX_I	29	input for stereo decoder (input impedance typ. 180 kΩ)
ST-LED	30	stereo indicator
LPF-M/S	31	pin for loop-filter and mono/stereo switch
MUTE	32	mute pin

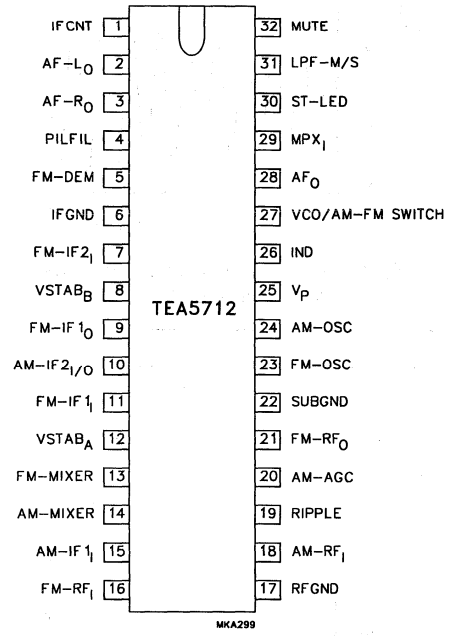


Fig.2 Pin configuration; TEA5712.

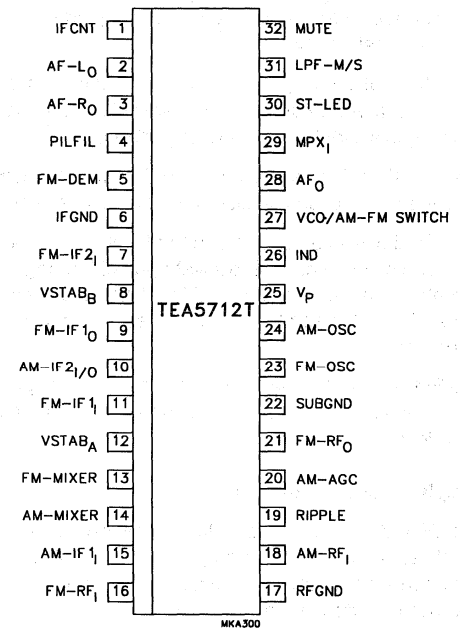


Fig.3 Pin configuration; TEA5712T.

FUNCTIONAL DESCRIPTION

The AM circuit incorporates a double balanced mixer, a one pin low-voltage oscillator (up to 30 MHz) a field-strength indicator output and is designed for distributed selectivity.

The AM input is designed to be connected to the top of a tuned circuit. AGC controls the IF amplification and for large signals it lowers the input impedance.

The first AM selectivity can be an IFT as well as an IFT combined with a ceramic filter; the second one is an IFT.

The FM circuit incorporates a tuned RF stage, a double balanced mixer, a one-pin oscillator, a field-strength indicator output and is designed for distributed IF ceramic filters. The FM quadrature detector uses a ceramic resonator.

The PLL stereo decoder incorporates a signal dependent stereo circuit, a soft-mute circuit and a stereo indicator LED driver.

Supply voltage behaviour

The TEA5712 incorporates internal stabilized power supplies. The maximum supply voltage is 12 V, the minimum voltage can go down temporarily to 1.8 V without any loss in performance.

Due to the capacitor at pin 19 (RIPPLE) the IC gives excellent performance, even when the actual supply voltage at pin 25 (V_P) drops below the voltage at pin 19 (RIPPLE).

Figures 4, 5 and 6 show that V_{stab}, which is dominant for the overall IC performance, remains unaffected, even if V_P drops down to 1.8 V or less. In this typical example the static or average V_P is equal to 2.5 V. Dips in V_{stab} appear only when the peak-to-peak value of the AC-component of $V_P > 2$ V, i.e. when the dynamic value of V_P drops down to 1.5 V for a short moment.

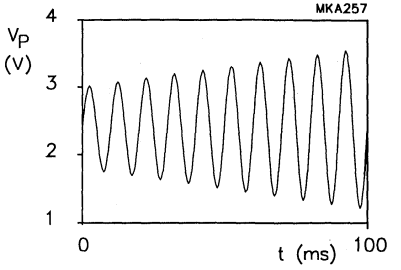


Fig.4 Supply voltage behaviour; V_P as a function of time.

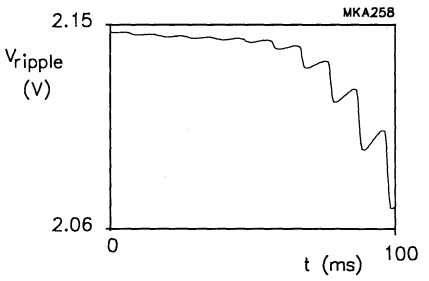


Fig.5 Supply voltage behaviour; V_{ripple} as a function of time.

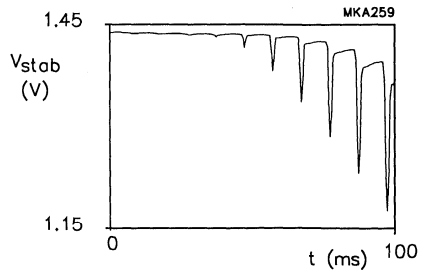


Fig.6 Supply voltage behaviour; V_{stab} as a function of time.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	0	12	V
T_{stg}	storage temperature	−55	+150	°C
T_{amb}	operating ambient temperature	−15	+60	°C
T_j	junction temperature	−15	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SDIP32	54	K/W
	SO32	68	K/W

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage		2.5	–	12	V
V_{CC2}	supply voltage for tuning		–	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC1}	supply current	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DD}	supply current	AM mode	–	3.3	–	mA
		FM mode	–	2.7	–	mA
I_{CC2}	supply current for tuning in preset mode (band-end to band-end)		–	–	640	µA
T_{amb}	operating ambient temperature		–15	–	+60	°C
AM performance; note 1						
V_{10}	AF output voltage	V_{i1} = 5 mV	36	45	70	mV
V_{i1}	RF sensitivity input voltage	S/N = 26 dB	40	55	70	µV
THD	total harmonic distortion	V_{i1} = 1 mV	–	0.8	2.0	%
FM performance; note 2						
V_{10}	AF output voltage	V_{i5} = 5 mV	40	48	57	mV
V_{i5}	RF sensitivity input voltage	V_{10} = –3 dB; V_{10} = 0 dB at V_{i5} = 1 mV	0.4	1.2	3.8	µV
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A	–	0.3	0.8	%
MPX performance; note 3						
α_{cs}	channel separation		26	30	–	dB

Notes

1. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 1 MHz; m = 0.3; f_m = 1 kHz; measured in Fig.9 with S1 in position A; S2 in position B; unless otherwise specified.
2. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 100 MHz; Δf_m = 22.5 kHz; f_m = 1 kHz; measured in Fig.9 with S2 in position A; S3 in position A and S5 in position A; unless otherwise specified.
3. V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; $V_{in3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; f_i = 1 kHz; measured in Fig.9 with S2 in position B; S3 in position B; unless otherwise specified.

BLOCK DIAGRAM

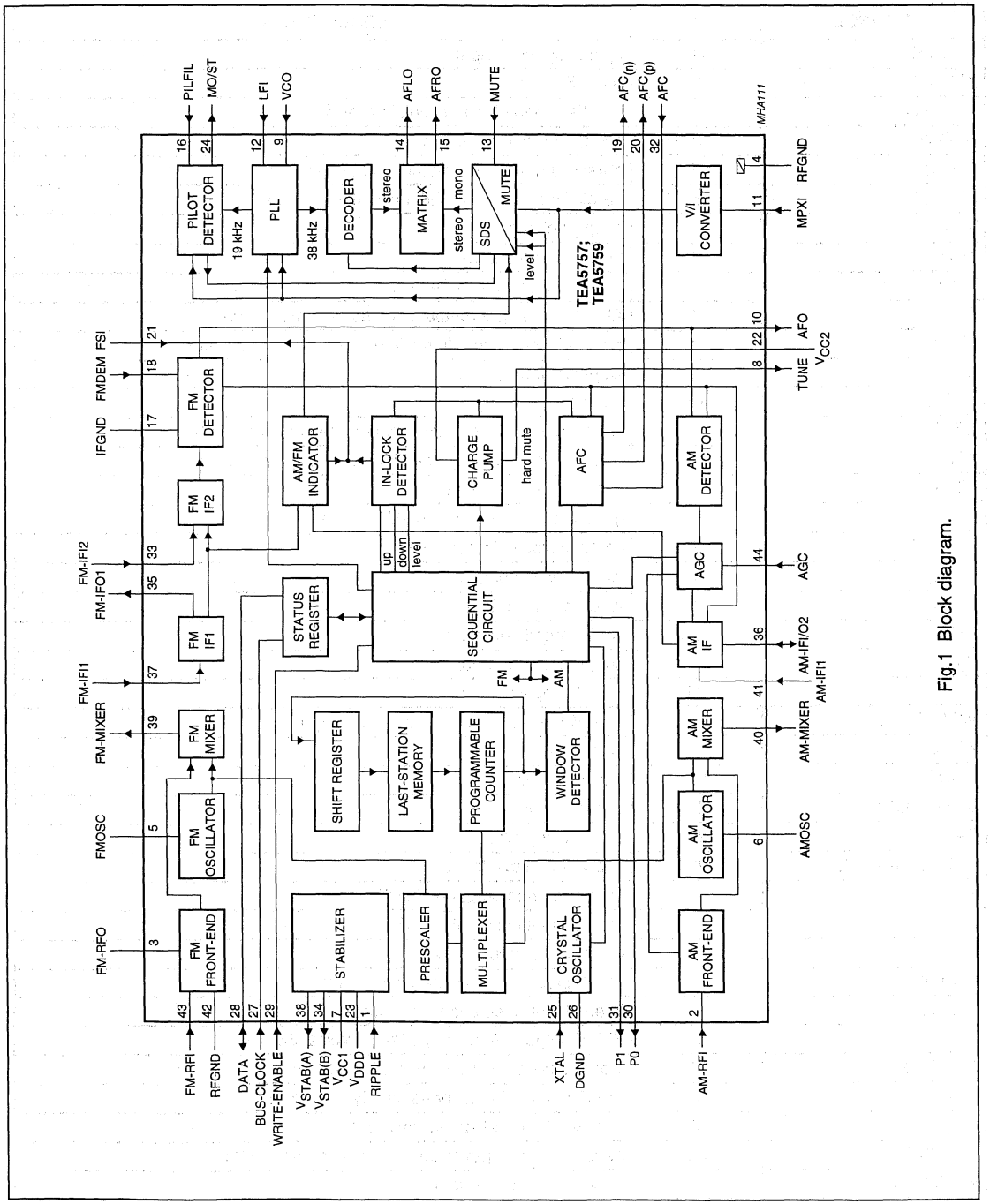


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor input
AM-RFI	2	AM-RF input
FM-RFO	3	parallel tuned FM-RF circuit to ground
RFGND	4	RF ground and substrate
FMOSC	5	parallel tuned FM-oscillator circuit to ground
AMOSC	6	parallel tuned AM-oscillator circuit to ground
V_{CC1}	7	supply voltage
TUNE	8	tuning output current
VCO	9	voltage controlled oscillator input
AFO	10	AM/FM AF output (output impedance typical 5 kΩ)
MPXI	11	stereo decoder input (input impedance typical 150 kΩ)
LFI	12	loop-filter input
MUTE	13	mute input
AFLO	14	left channel output (output impedance typical 4.3 kΩ)
AFRO	15	right channel output (output impedance typical 4.3 kΩ)
PILFIL	16	pilot detector filter input
IFGND	17	ground of IF, detector and MPX stage
FMDEM	18	ceramic discriminator input
$AFC_{(n)}$	19	AFC negative output
$AFC_{(p)}$	20	AFC positive output
FSI	21	field-strength indicator
V_{CC2}	22	supply voltage for tuning
V_{DDD}	23	digital supply voltage
MO/ST	24	mono/stereo and tuning indication output
XTAL	25	crystal input
DGND	26	digital ground
BUS-CLOCK	27	bus-clock input
DATA	28	bus data input/output
WRITE-ENABLE	29	bus write-enable input
P0	30	programmable output port (P0)
P1	31	programmable output port (P1)
AFC	32	450 kHz LC-input circuit
FM-IFI2	33	FM-IF input 2 (input impedance typical 330 Ω)
$V_{STAB(B)}$	34	internal stabilized supply voltage (B)
FM-IFO1	35	FM-IF output 1 (input impedance typical 330 Ω)
AM-IFI/O2	36	input/output to IFT; output: current source
FM-IFI1	37	FM-IF input 1 (input impedance typical 330 Ω)
$V_{STAB(A)}$	38	internal stabilized supply voltage (A)
FM-MIXER	39	ceramic filter output (output impedance typical 330 Ω)
AM-MIXER	40	open-collector output to IFT

SYMBOL	PIN	DESCRIPTION
AM-IFI1	41	IFT or ceramic filter input (input impedance typical 3 kΩ)
RFGND	42	FM-RF ground
FM-RFI	43	FM-RF aerial input (input impedance typical 40 Ω)
AGC	44	AGC capacitor input

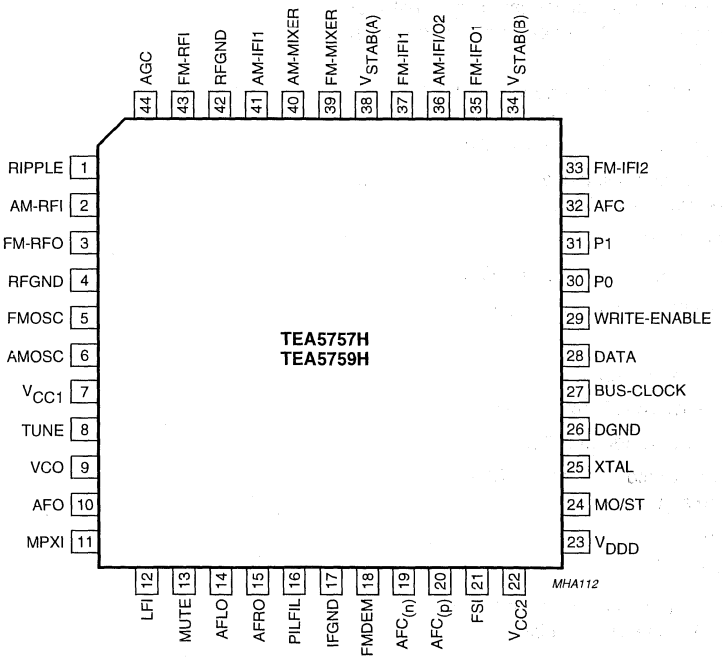


Fig.2 Pin configuration.

Self tuned radio TEA5762

FEATURES

- The tuning system has an optimized IC partitioning both from application (omitting interferences) and flexibility (removable front panel option) point of view: the tuning synthesizer is on-chip with the radio
- The tuning quality is superior and requires no IF counter for stop-detection; it is insensitive to ceramic filter tolerances
- In combination with the microcontroller, fast, low-power operation of preset mode, manual search, automatic search and automatic store are possible
- The local (internal) controller function facilitates reduced and simplified microcontroller software
- The high integration level means fewer external components with regard to the communication between the radio and the microcontroller and a simple and small printed-circuit board (PCB)
- The inherent FUZZY LOGIC behaviour of STR (Self Tuned Radio), which mimics hand tuning, yields a potentially fast yet reliable tuning operation
- The level of the incoming signal at which the radio must lock is software programmable
- Two programmable ports
- FM-on/off port to control the external FM front end
- High selectivity with distributed IF gain
- Soft mute
- Signal dependent stereo-blend
- High impedance MOSFET input on AM
- Wide supply voltage range of 2.5 to 12 V
- Low current consumption 18 mA at AM and FM (including tuning synthesizer for AM)
- Low noise figure
- Low output distortion
- Due to the new tuning concept, the tuning is independent of the channel spacing.

GENERAL DESCRIPTION

The TEA5762 is a 44-pin integrated AM-radio and FM-IF and demodulator part including a novel tuning concept. The radio part is based on the TEA5712.

It is designed for the use with an external FM-front end.

The new tuning concept combines the advantages of hand tuning with electronic facilities and features. User intelligence is incorporated into the tuning algorithm and an improvement of the analog signal processing is used for the AFC function.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5762H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage 1		2.5	–	12	V
V_{CC2}	supply voltage 2 for tuning		–	–	12	V
V_{tune}	tuning voltage		0.7	–	$V_{CC2} - 0.75$	V
I_{CC1}	supply current 1	AM mode	12	15	18	mA
		FM mode	13	16	19	mA
I_{DDD}	digital supply current	AM mode	–	3.3	–	mA
		FM mode	–	2.7	–	mA
I_{CC2}	supply current 2 for tuning in preset mode (band-end to band-end)		–	–	640	µA
T_{amb}	operating ambient temperature		–15	–	+60	°C
AM performance; note 1						
V_{10}	AF output voltage	V_{i1} = 5 mV	36	45	70	mV
V_{i1}	RF sensitivity input voltage	S/N = 26 dB	40	55	70	µV
THD	total harmonic distortion	V_{i1} = 1 mV	–	0.8	2.0	%
FM performance; note 2						
V_{10}	AF output voltage	V_{i4} = 5 mV	40	48	57	mV
V_{i4}	IF sensitivity input voltage	V_{10} = –3 dB; V_{10} = 0 dB at V_{i4} = 10 mV	–	20	30	µV
THD	total harmonic distortion	IF filter SFE10.7MS3A20K-A	–	0.3	0.8	%
MPX performance; note 3						
α_{cs}	channel separation	V_{i4} = 30 mV	26	30	–	dB

Notes

1. Conditions AM: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 1 MHz; m = 0.3; f_m = 1 kHz; measured in Fig.8 with S1 in position A and S2 in position B; unless otherwise specified.
2. Conditions FM: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; f_i = 10.7 MHz; Δf_m = 22.5 kHz; f_m = 1 kHz; measured in Fig.8 with S2 in position A and S3 in position A; unless otherwise specified.
3. Conditions MPX: V_{CC1} = 3 V; V_{CC2} = 12 V; V_{DDD} = 3 V; $V_{i3(L+R)}$ = 155 mV; V_{pilot} = 15.5 mV; f_i = 1 kHz; measured in Fig.8 with S2 in position B and S3 in position B; unless otherwise specified.

BLOCK DIAGRAM

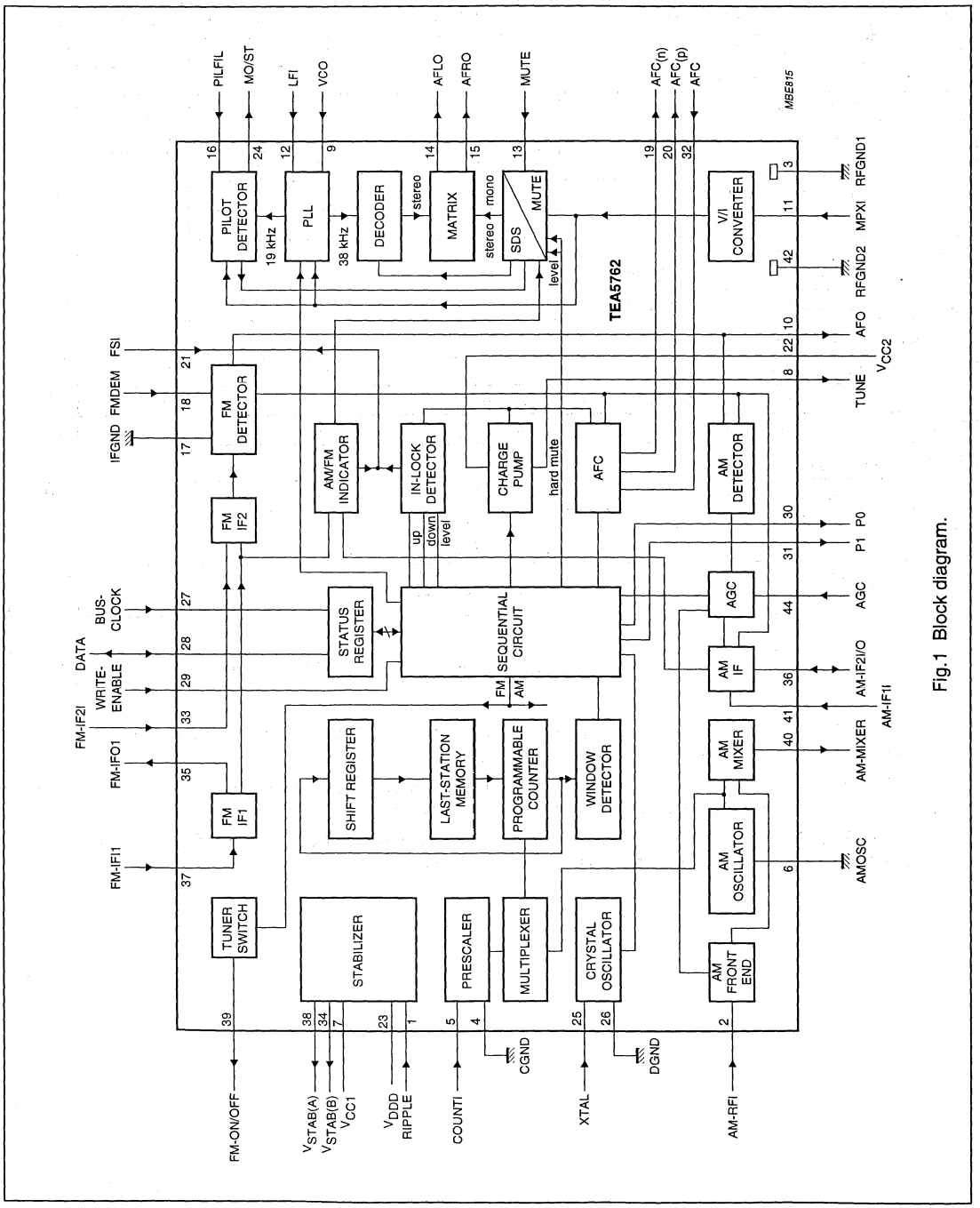


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RIPPLE	1	ripple capacitor input
AM-RFI	2	AM-RF input
RFGND1	3	RF ground 1 and substrate
CGND	4	counter ground
COUNTI	5	counter input
AMOSC	6	parallel tuned AM oscillator circuit to ground
V_{CC1}	7	supply voltage 1
TUNE	8	tuning output current
VCO	9	voltage controlled oscillator input
AFO	10	AM/FM AF output (output impedance typical 5 kΩ)
MPXI	11	stereo decoder input (input impedance typical 150 kΩ)
LFI	12	loop-filter input
MUTE	13	mute input
AFLO	14	left channel output (output impedance typical 4.3 kΩ)
AFRO	15	right channel output (output impedance typical 4.3 kΩ)
PILFIL	16	pilot detector filter input
IFGND	17	ground of IF, detector and MPX stage
FMDEM	18	ceramic discriminator input
$AFC_{(n)}$	19	AFC negative output
$AFC_{(p)}$	20	AFC positive output
FSI	21	field-strength indicator
V_{CC2}	22	supply voltage 2 (for tuning)
V_{DDD}	23	digital supply voltage
MO/ST	24	mono/stereo and tuning indication output
XTAL	25	crystal input
DGND	26	digital ground
BUS-CLOCK	27	bus-clock input
DATA	28	bus data input/output
WRITE-ENABLE	29	bus write enable input
P0	30	programmable output port (P0)
P1	31	programmable output port (P1)
AFC	32	450 kHz LC input circuit for AM AFC
FM-IF2I	33	FM-IF input 2 (input impedance typical 330 Ω)
$V_{STAB(B)}$	34	internal stabilized supply voltage (B)
FM-IFO1	35	FM-IF output 1 (input impedance typical 330 Ω)
AM-IF2I/O	36	input/output to IFT; output current source
FM-IFI1	37	FM-IF input 1 (input impedance typical 330 Ω)
$V_{STAB(A)}$	38	internal stabilized supply voltage (A)
FM-ON/OFF	39	FM ON/OFF port
AM-MIXER	40	open-collector output to IFT

SYMBOL	PIN	DESCRIPTION
AM-IF1I	41	IFT or ceramic filter input (input impedance typical 3 kΩ)
RFGND2	42	FM-RF ground 2
n.c.	43	not connected
AGC	44	AGC capacitor input

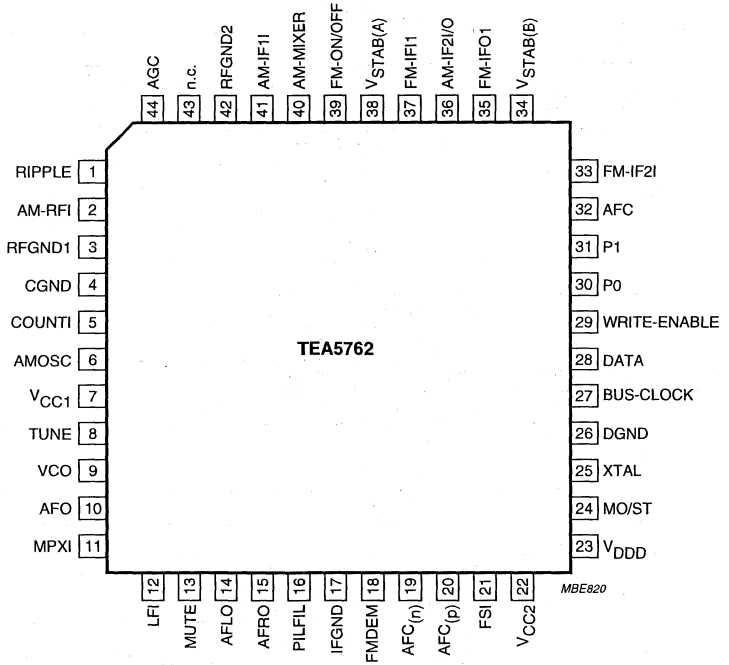


Fig.2 Pin configuration.

Sound fader control circuit TEA6320

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6320 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−15	–	+15	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	76	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6320	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
TEA6320T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

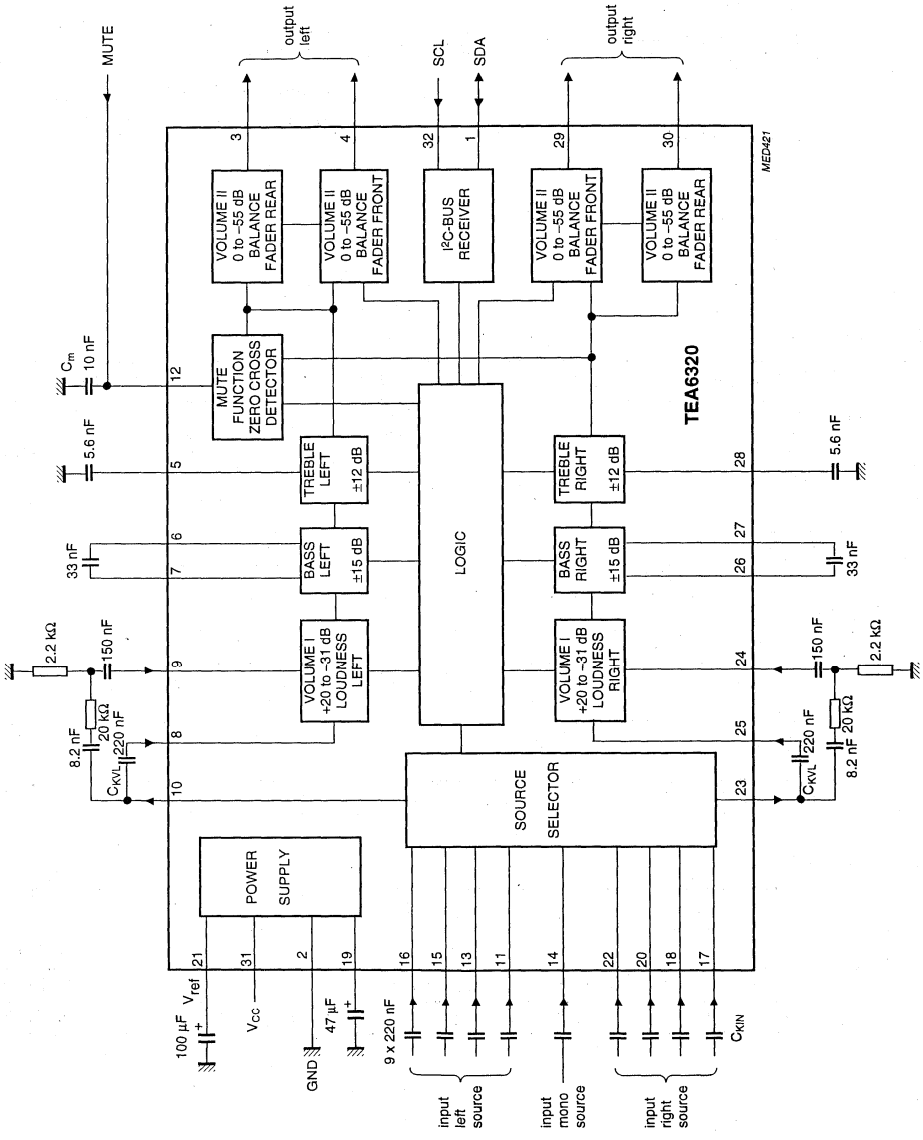


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control capacitor left channel or output to an external equalizer
B1L	7	bass control capacitor, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control capacitor right channel
B2R	27	bass control capacitor right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

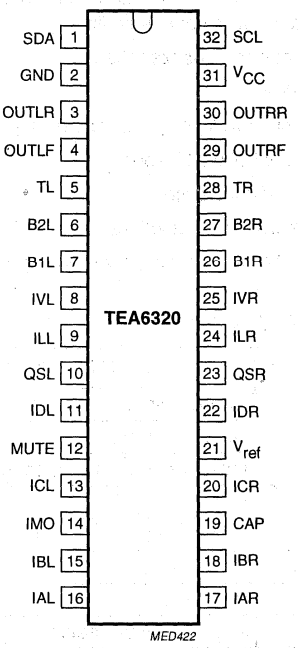


Fig.2 Pin configuration.

Sound fader control circuit TEA6321

FEATURES

- Source selector for four stereo and one mono inputs
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset.

GENERAL DESCRIPTION

The sound fader control circuit TEA6321 is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		−86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−18	–	+18	dB
G_{treble}	treble control		−12	–	+12	dB
$G_{step(treble)}$	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
α_{cs}	channel separation	250 Hz ≤ f ≤ 10 kHz; G_v = 0 dB	90	96	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6321T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

BLOCK DIAGRAM

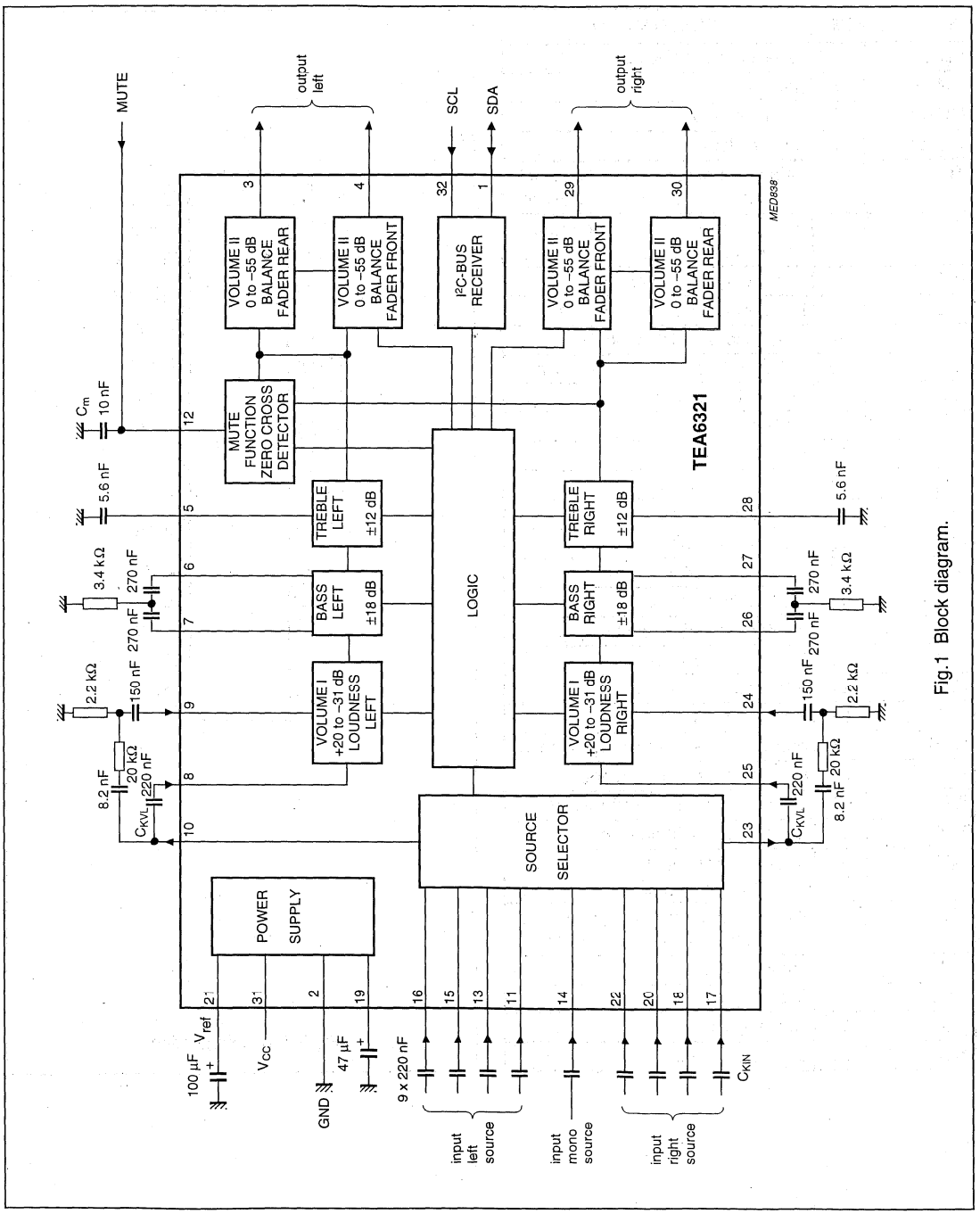


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
GND	2	ground
OUTLR	3	output left rear
OUTLF	4	output left front
TL	5	treble control capacitor left channel or input from an external equalizer
B2L	6	bass control left channel or output to an external equalizer
B1L	7	bass control, left channel
IVL	8	input volume I, left control part
ILL	9	input loudness, left control part
QSL	10	output source selector, left channel
IDL	11	input D left source
MUTE	12	mute control
ICL	13	input C left source
IMO	14	input mono source
IBL	15	input B left source
IAL	16	input A left source
IAR	17	input A right source
IBR	18	input B right source
CAP	19	electronic filtering for supply
ICR	20	input C right source
V_{ref}	21	reference voltage ($0.5V_{CC}$)
IDR	22	input D right source
QSR	23	output source selector right channel
ILR	24	input loudness right channel
IVR	25	input volume I, right control part
B1R	26	bass control right channel
B2R	27	bass control right channel or output to an external equalizer
TR	28	treble control capacitor right channel or input from an external equalizer
OUTRF	29	output right front
OUTRR	30	output right rear
V_{CC}	31	supply voltage
SCL	32	serial clock input

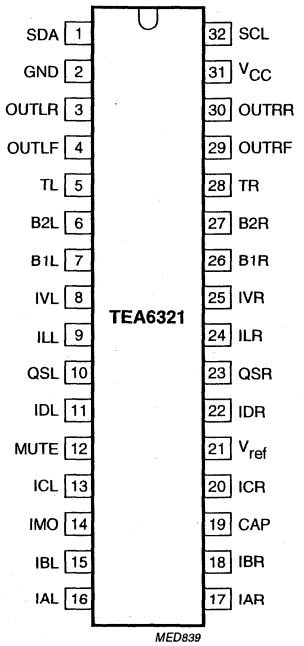


Fig.2 Pin configuration.

Sound fader control circuit TEA6322T

FEATURES

- Source selector for three stereo and one differential stereo input for remote sources
- The differential stereo input works optional as a fourth stereo input and the common mode pin can be used as well as an additional mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Output at volume I for external booster
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Mute control at audio signal zero crossing
- Logic output to read mute status
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset
- Power-down indication.

GENERAL DESCRIPTION

The sound fader control circuit TEA6322T is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8.5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–15	–	+15	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (bass, treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6322T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

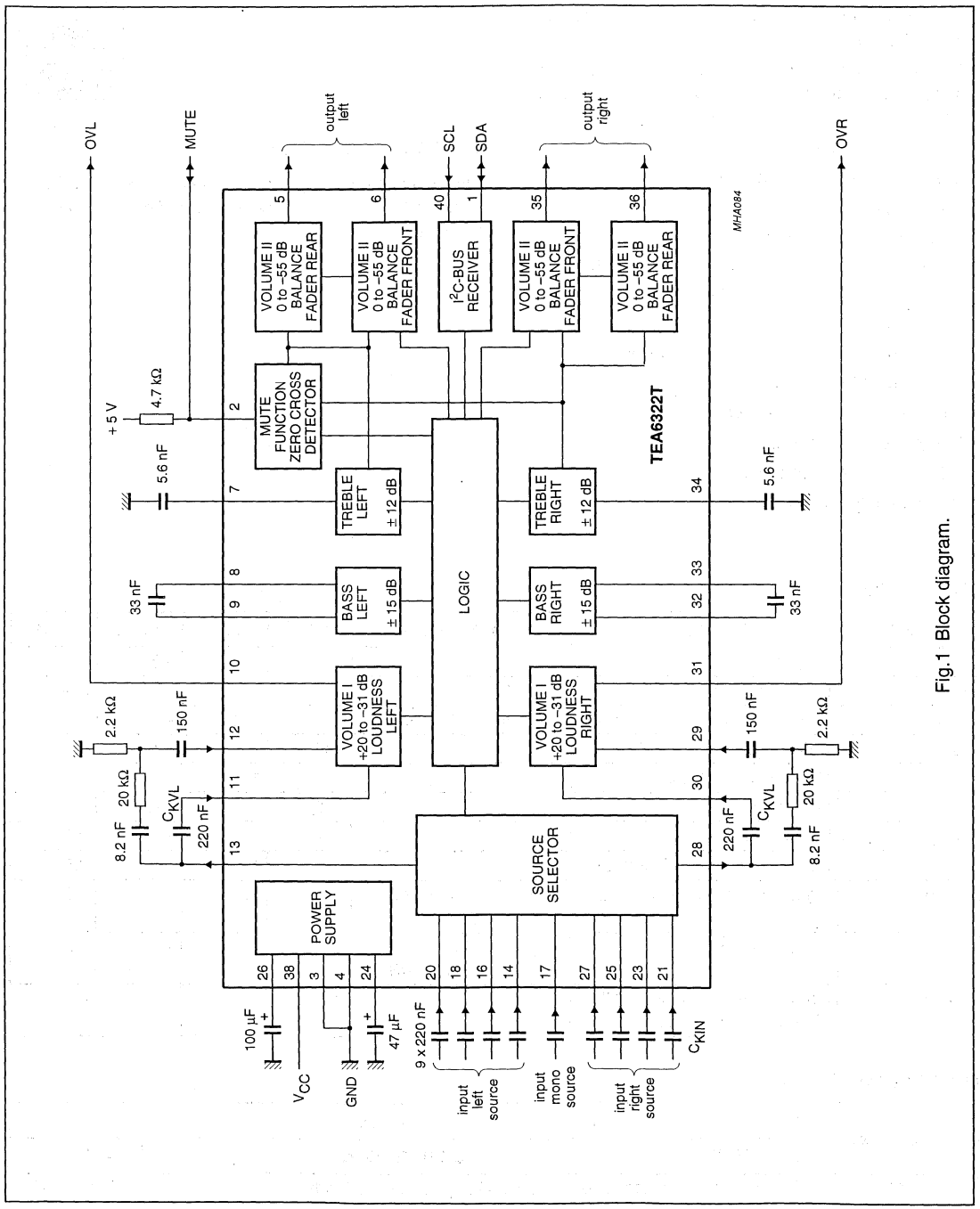


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
MUTE	2	mute control input and output
DGND	3	digital ground
AGND	4	analog ground
OUTLR	5	output left rear
OUTLF	6	output left front
TL	7	treble control capacitor left channel or input from external equalizer
B2L	8	bass control capacitor left channel or output to an external equalizer
B1L	9	bass control capacitor, left channel
OVL	10	output volume I, left channel
IVL	11	input volume I, left control part
ILL	12	input loudness, left control part
QSL	13	output source selector, left channel
IDL	14	input D left source
i.c.	15	COMM, common mode rejection adjust, centre position
ICL	16	input C left source
COM	17	common mode input / mono source input
IBL	18	input B left source
i.c.	19	COML, common mode rejection adjust, left position
IAL	20	input A differential source left
IAR	21	input A differential source right
i.c.	22	COMR, common mode rejection adjust, right position
IBR	23	input B right source
CAP	24	electronic filtering for supply
ICR	25	input C right source
V_{ref}	26	reference voltage (0.5 V_{CC})
IDR	27	input D right source
QSR	28	output source selector right channel
ILR	29	input loudness right channel
IVR	30	input volume I, right control part
OVR	31	output volume I, right channel
B1R	32	bass control capacitor right channel
B2R	33	bass control capacitor right channel or output to an external equalizer
TR	34	treble control capacitor right channel or input from an external equalizer
OUTRF	35	output right front
OUTRR	36	output right rear
n.c.	37	not connected
V_{CC}	38	supply voltage
n.c.	39	not connected
SCL	40	serial clock input

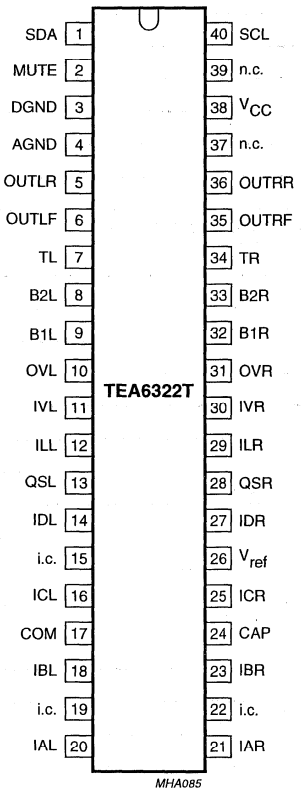


Fig.2 Pin configuration.

Sound fader control circuit TEA6323T

FEATURES

- Source selector for three stereo and one differential stereo input for remote sources
- The differential stereo input works optional as a fourth stereo input and the common mode pin can be used as well as an additional mono input
- Interface for noise reduction circuits
- Interface for external equalizer
- Volume, balance and fader control
- Output at volume I for external booster
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass control with equalizer filters
- Treble control
- Mute control at audio signal zero crossing
- Logic output to read mute status
- Fast mute control via I²C-bus
- Fast mute control via pin
- I²C-bus control for all functions
- Power supply with internal power-on reset
- Power down indication.

GENERAL DESCRIPTION

The sound fader control circuit TEA6323T is an I²C-bus controlled stereo preamplifier for car radio hi-fi sound applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.5	8.5	9.5	V
I_{CC}	supply current	V_{CC} = 8:5 V	–	26	–	mA
$V_{o(rms)}$	maximum output voltage level	V_{CC} = 8.5 V; THD ≤ 0.1%	–	2000	–	mV
G_v	voltage gain		–86	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		–18	–	+18	dB
G_{treble}	treble control		–12	–	+12	dB
$G_{step(treble)}$	step resolution (treble)		–	1.5	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_O = 2.0 V; G_v = 0 dB; unweighted	–	105	–	dB
RR_{100}	ripple rejection	$V_{r(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	75	–	dB
CMRR	common mode rejection ratio differential stereo input		43	53	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6323T	VSO40	plastic very small outline package; 40 leads	SOT158-1

BLOCK DIAGRAM

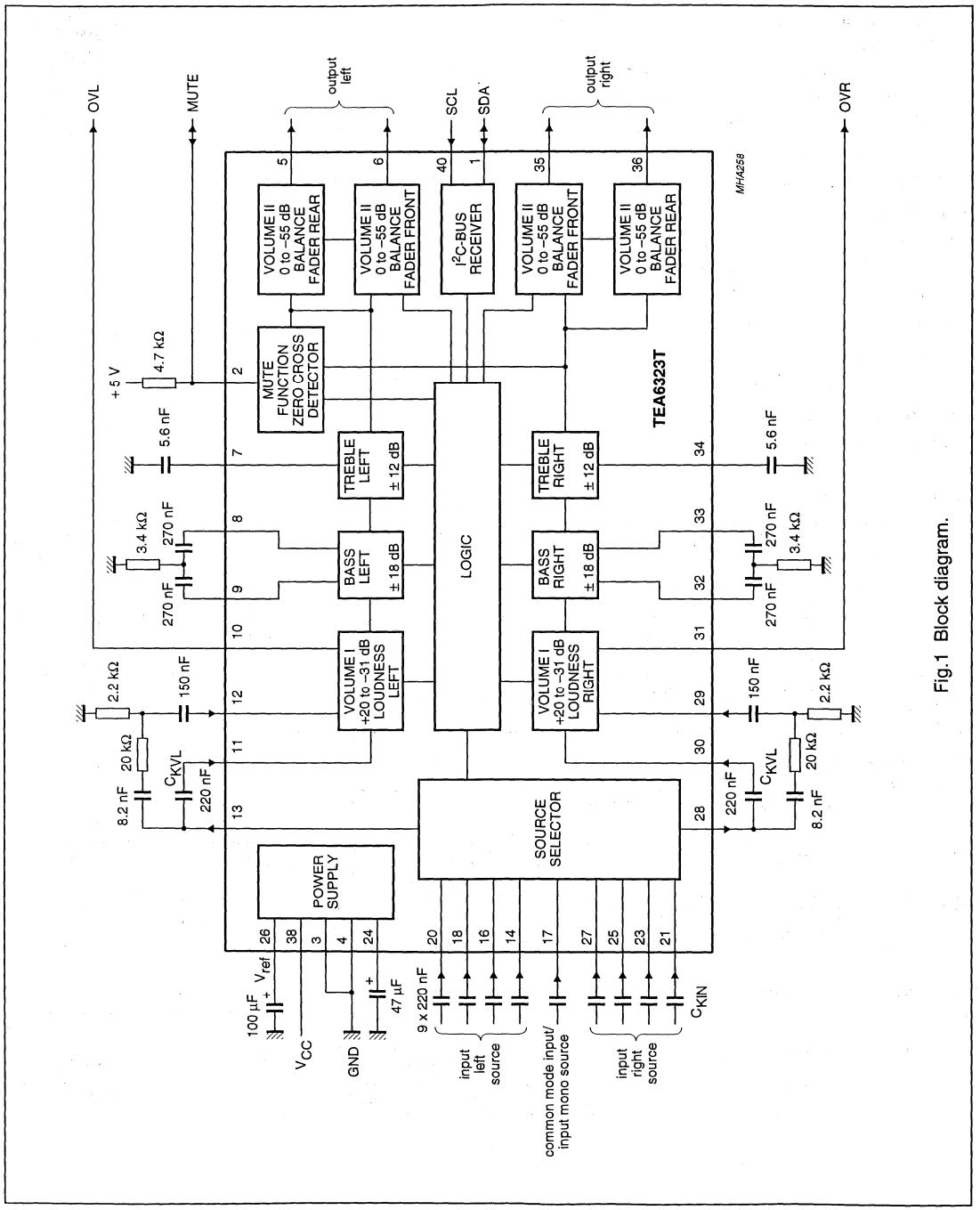


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	serial data input/output
MUTE	2	mute control input and output
DGND	3	digital ground
AGND	4	analog ground
OUTLR	5	output left rear
OUTLF	6	output left front
TL	7	treble control capacitor left channel or input from an external equalizer
B2L	8	bass control left channel or output to an external equalizer
B1L	9	bass control, left channel
OVL	10	output volume I, left channel
IVL	11	input volume I, left control part
ILL	12	input loudness, left control part
QSL	13	output source selector, left channel
IDL	14	input D left source
i.c.	15	COMM, common mode rejection adjust, centre position
ICL	16	input C left source
COM	17	common mode input / mono source input
IBL	18	input B left source
i.c.	19	COML, common mode rejection adjust, left position
IAL	20	input A differential source left
IAR	21	input A differential source right
i.c.	22	COMR, common mode rejection adjust, right position
IBR	23	input B right source
CAP	24	electronic filtering for supply
ICR	25	input C right source
V_{ref}	26	reference voltage ($0.5V_{CC}$)
IDR	27	input D right source
QSR	28	output source selector right channel
ILR	29	input loudness right channel
IVR	30	input volume I, right control part
OVR	31	output volume I, right channel
B1R	32	bass control right channel
B2R	33	bass control right channel or output to an external equalizer
TR	34	treble control capacitor right channel or input from an external equalizer
OUTRF	35	output right front
OUTRR	36	output right rear
n.c.	37	not connected
V_{CC}	38	supply voltage
n.c.	39	not connected
SCL	40	serial clock input

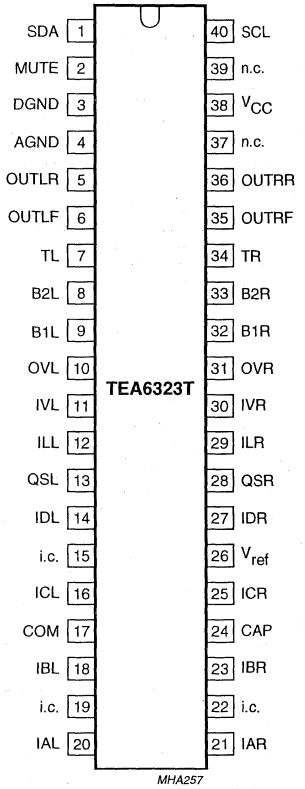


Fig.2 Pin configuration.

Front-end and PLL synthesizers for car radios

TEA6810V; TEA6811V

FEATURES

- Synthesizer function which includes a Voltage Controlled Oscillator (VCO), dividers, phase detector, charge-pump and in-lock detector
- FM mixer with AGC
- AM RF amplifier with AGC
- AM mixer.

APPLICATIONS

- Car radios.

GENERAL DESCRIPTION

The TEA6810V and TEA6811V, together with TEA6821V forms an AM/FM receiving concept for electronically tuned car radios.

The TEA681xV is an FM/AM front-end with one local synthesized oscillator for both AM and FM which is used together with the TEA6821T in a double-conversion concept. It delivers a first FM-IF of 72.2 MHz and, for MW/LW, a first AM-IF of 10.7 MHz.

Minimum alignments are required due to wideband RF inputs and the common AM/FM VCO.

High dynamic behaviour and minimum distortion is obtained by a special RF input design combined with AGC. High sensitivity is possible in combination with RF input FETs.

Minimum interference is experienced due a to special synthesizer loop design and ensuring that the I²C-bus is inoperative in the locked-tuned condition.

The reference frequency for the synthesizer and the I²C-bus information is delivered by the TEA6821V.

The programmable local/dx switch enables switching the gain of the FM mixer from normal AGC control (FM dx) to the forced 4th level of AGC (FM local).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA1}	analog supply voltage (pin 2)		4.75	5.0	5.25	V
V_{CCA2}	analog supply voltage (pin 13)		8.1	8.5	8.9	V
V_{AMant}	AM AGC range	see Fig.4	0.3	–	6.0	V
V_{FMant}	FM AGC range	see Fig.5	10	–	600	mV
f_{AMant}	AM input frequency		0.144	–	22	MHz
f_{FMant}	FM input frequency		60	–	108	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6810V	VSO40	plastic very small outline package; 40 leads	SOT158-1
TEA6811V	VSO40	plastic very small outline package; 40 leads; face down	SOT158-2

BLOCK DIAGRAM

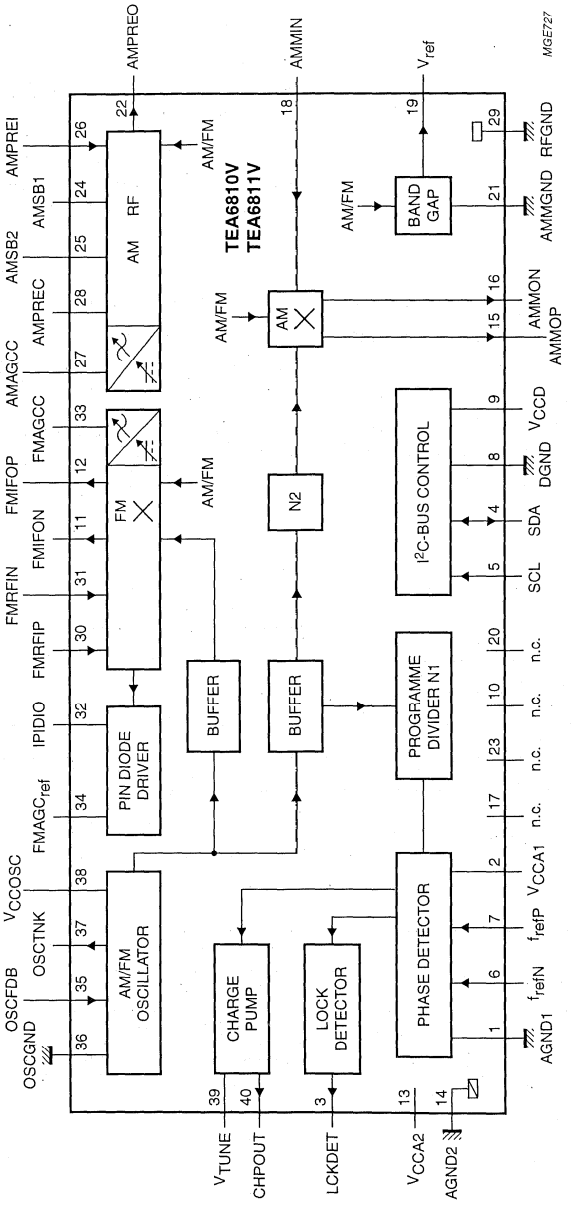


Fig.1 Block diagram.

PINNING

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
AGND1	1	1	analog ground 1
V_{CCA1}	2	2	analog supply voltage 1 (+5 V)
LCKDET	3	3	lock detector flag
SDA	4	4	serial data input/output; I^2C-bus
SCL	5	5	serial clock input; I^2C-bus
f_{refN}	6	6	reference frequency input from TEA6821 N-terminal
f_{refP}	7	7	reference frequency input from TEA6821 P-terminal
DGND	8	8	digital ground
V_{CCD}	9	9	digital supply voltage (+5 V)
n.c.	10	10	not connected
FMIFON	11	11	FM mixer negative output (72.2 MHz)
FMIFOP	12	12	FM mixer positive output (72.2 MHz)
V_{CCA2}	13	13	analog supply voltage 2 (+8.5 V)
AGND2	14	14	analog ground 2
AMMOP	15	15	AM mixer positive output (10.7 MHz)
AMMON	16	16	AM mixer negative output (10.7 MHz)
n.c.	17	17	not connected
AMMIN	18	18	AM mixer RF input
V_{ref}	19	19	reference voltage output from AM band gap
n.c.	20	20	not connected
AMMGND	21	21	AM mixer ground
AMPREO	22	22	AM preamplifier output
n.c.	23	23	not connected
AMSB1	24	24	AM feedback switch SB1
AMSB2	25	25	AM feedback switch SB2
AMPREI	26	26	AM preamplifier input
AMAGCC	27	27	AM AGC capacitor
AMPREC	28	28	AM preamplifier decoupling capacitor
RFGND	29	29	RF ground
FMRFIP	30	30	RF positive input for FM mixer
FMRFIN	31	31	RF negative input for FM mixer
IPIDIO	32	32	pin diode drive
FMAGCC	33	33	FM AGC integrating capacitor
$FMAGC_{ref}$	34	34	FM AGC reference voltage
OSCFDB	35	35	oscillator feedback input
OSCGND	36	36	oscillator ground
OSCTNK	37	37	oscillator tank output

SYMBOL	PIN[1]		DESCRIPTION
	TEA6810	TEA6811	
V_{CCOSC}	38	38	oscillator supply voltage (+8.5 V)
V_{TUNE}	39	39	tuning voltage
CHPOUT	40	40	charge pump output

Note

1. Pins 10, 17, 20 and 23 should be connected to a common ground.

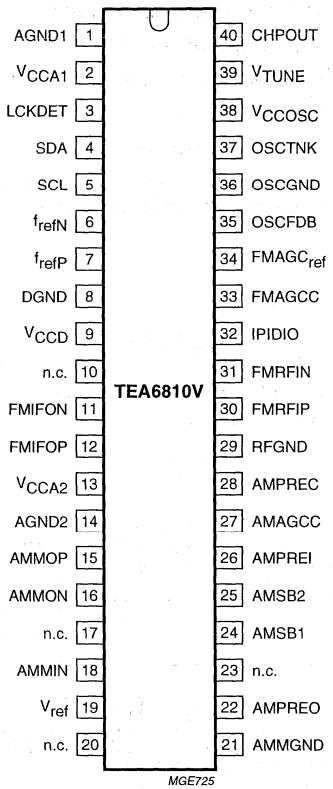


Fig.2 Pin configuration (TEA6810).

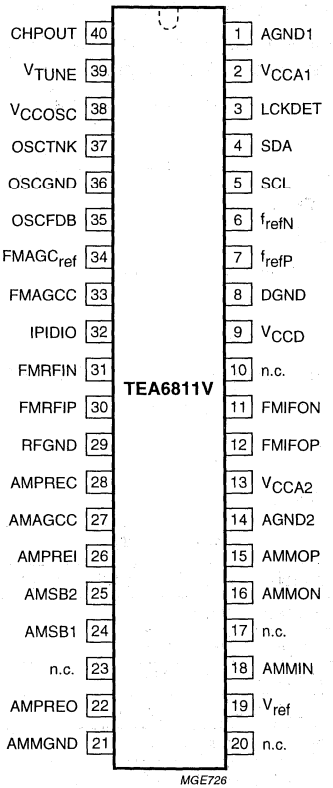


Fig.3 Pin configuration (TEA6811).

ICE car radio TEA6821T

FEATURES

General

- FM mixer for conversion from FM IF_1 = 72.2 MHz to FM IF_2 = 10.7 MHz
- AM mixer for conversion from AM IF_1 = 10.7 MHz to AM IF_2 = 450 kHz
- FM IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjust and THD compensation
- Level and multipath and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF amplifier and demodulator
- I^2C-bus transceiver
- IF count for AM and FM
- Reference frequency generation for PLL synthesizer
- Reduced external components
- SW applicable.

Stereo decoder

- Adjustment-free PLL-VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot canceller
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6821T together with the TEA6810T / TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept for European, American and Japanese frequency range.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{s1}	supply voltage 1 (pins 56 and 28)	note 1	7	8.5	10	V
V_{s1}	operating range		8.1	8.5	8.9	V
I_{s1}	supply current 1 FM		–	28	–	mA
I_{s1}	supply current 1 AM		–	24	–	mA
V_{s2}	supply voltage 2 (pin 5)	note 1	4.5	5.0	5.5	V
V_{s2}	operating range		4.75	5.0	5.25	V
I_{s2}	supply current 2 FM		–	31	–	mA
I_{s2}	supply current 2 AM		–	28	–	mA
S+N/N	signal-to-noise AM	m = 0.3	–	57	–	dB
THD	distortion AM		–	1	2	%
S+N/N	signal-to-noise FM	Δf = 22.5 kHz at pins 43 and 47	66	72	–	dB
THD	distortion FM	Δf = 75 kHz	–	0.1	0.35	%
α	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		–40	–	+85	°C

Note to the quick reference data

1. IC is functional, specified parameters may deviate from limits which are valid for operating range.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6821T	VSO56	plastic very small outline package; 56 leads	SOT190-1

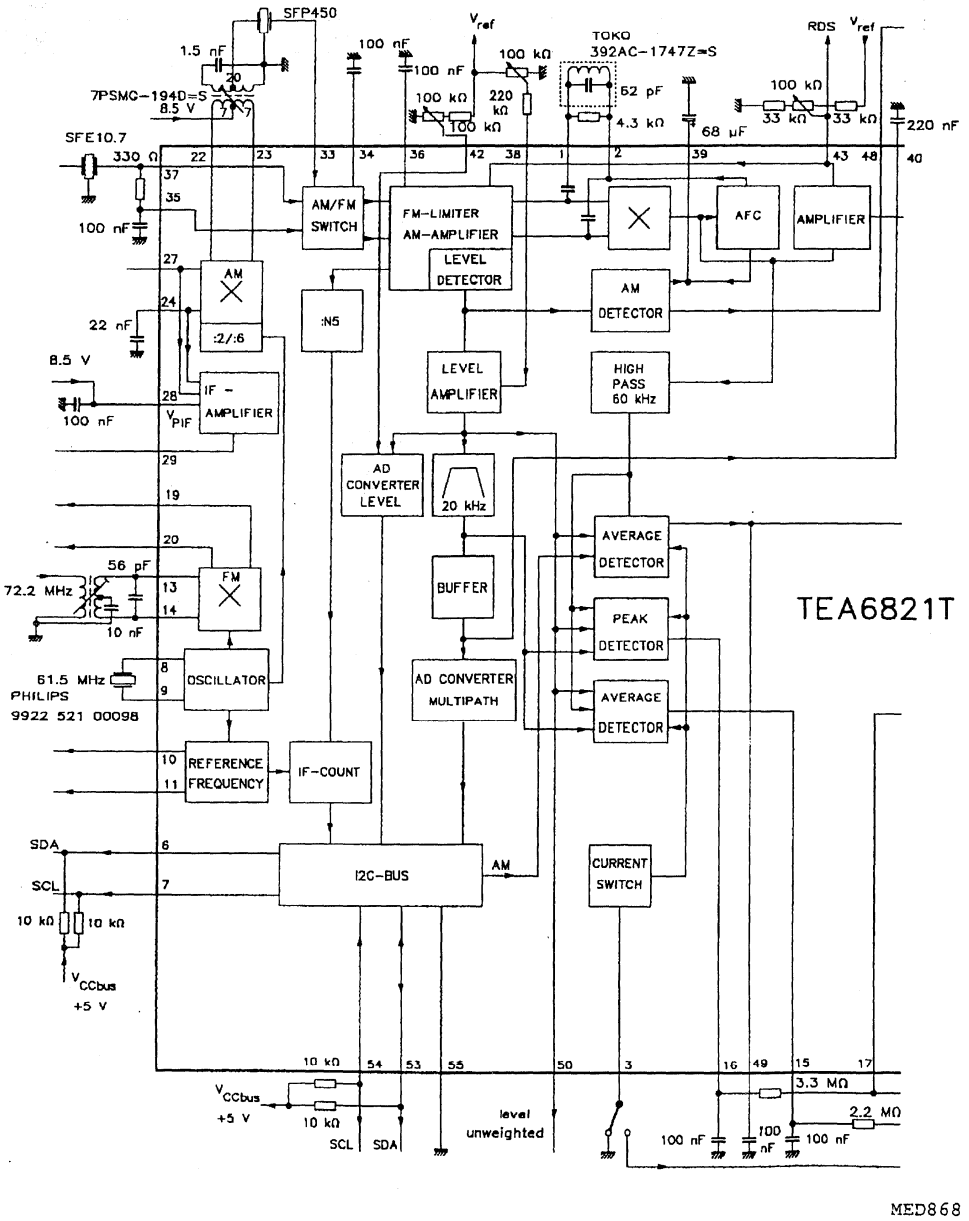


Fig.1 Block diagram (continued in Fig.2).

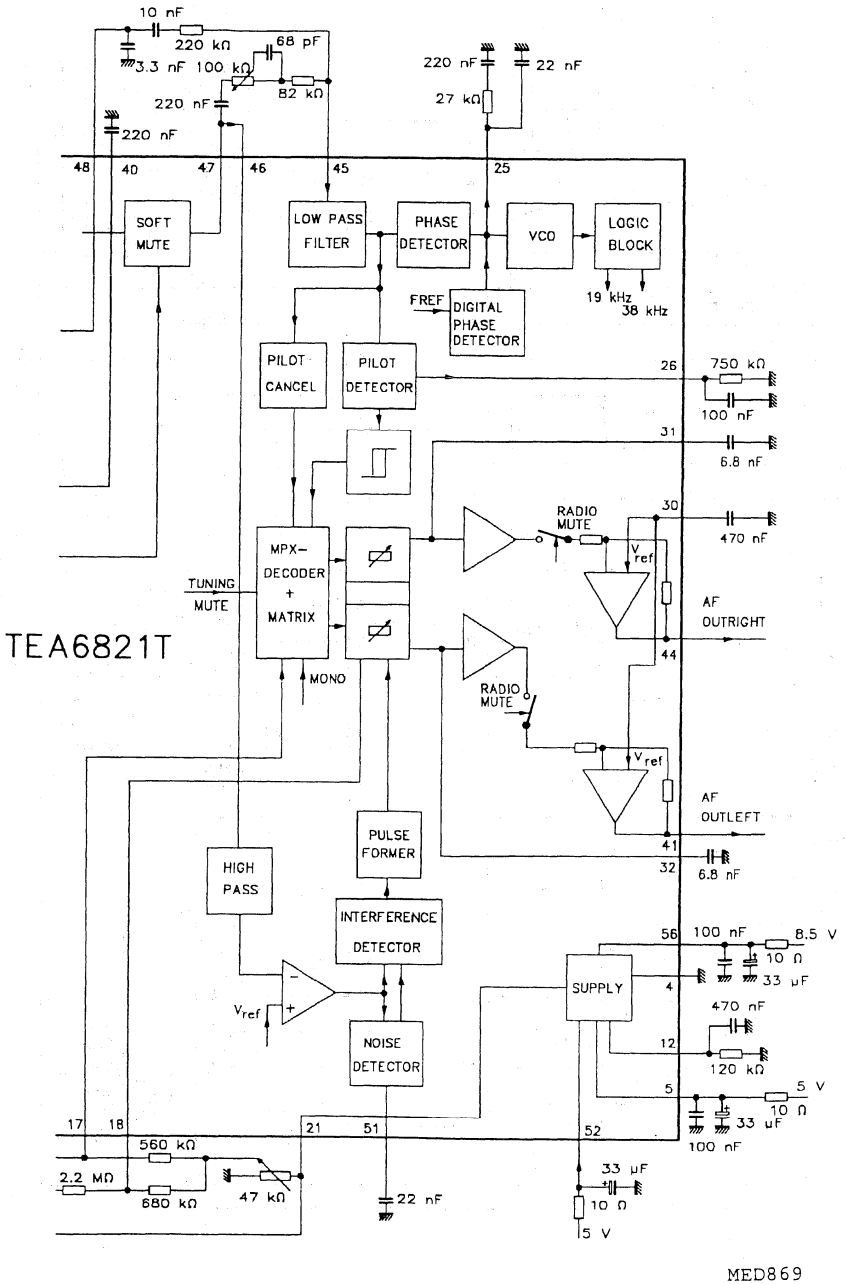


Fig.2 Block diagram (continued from Fig.1).

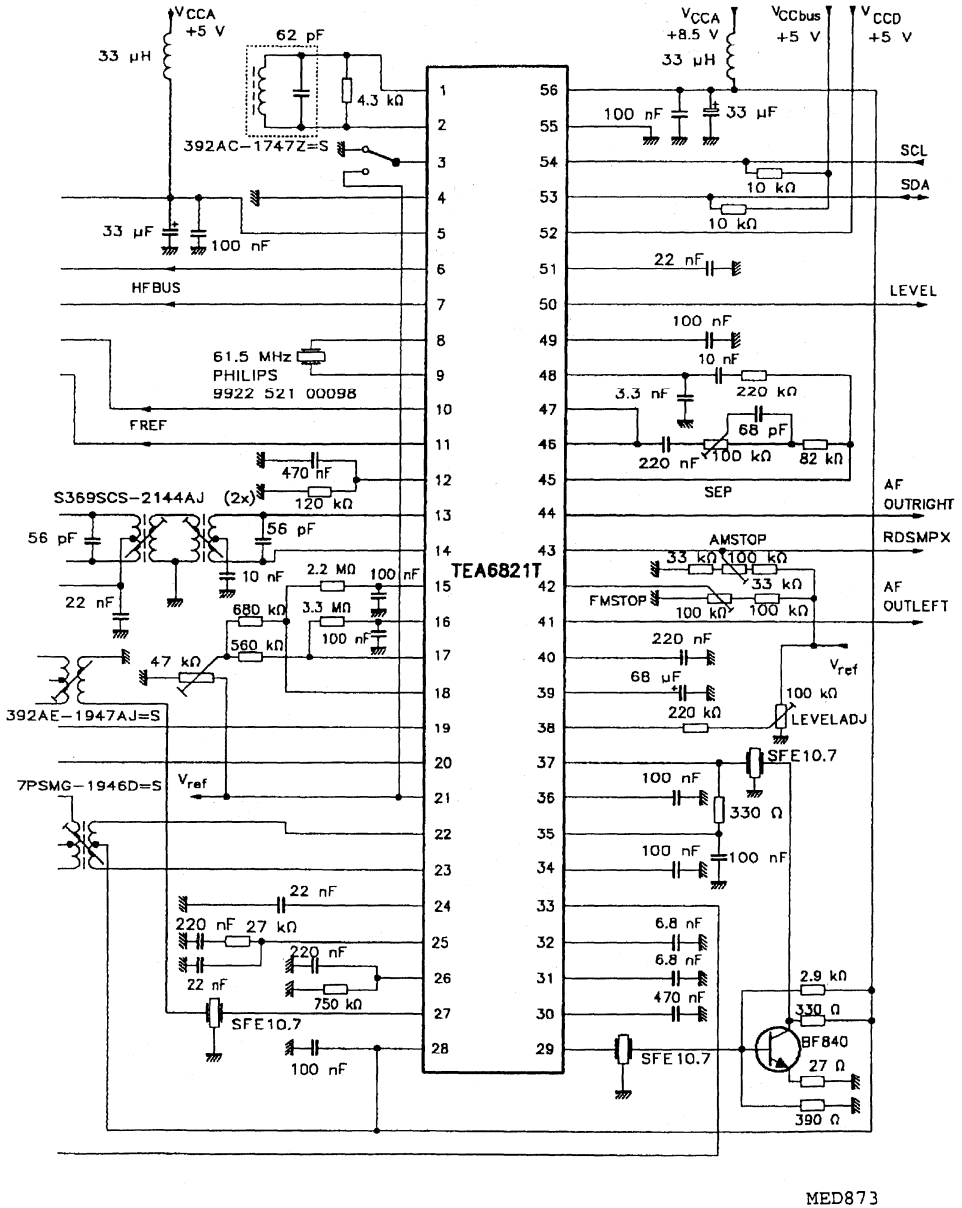


Fig.6 AM/FM car radio receiver with TEA6811T and TEA6821T (continued from Fig.5).

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank
QDET2	2	demodulator tank
TSWITCH	3	time switch
GND	4	analog ground
V_{P5}	5	5 V supply voltage
HFBUS1	6	HF bus, pull-up to 5 V
HFBUS2	7	HF bus, pull-up to 5 V
XTAL1	8	crystal oscillator
XTAL2	9	crystal oscillator
F_{REFP}	10	PLL reference frequency
F_{REFN}	11	PLL reference frequency
I_{REF}	12	reference current
FMIF1IN1	13	70 MHz FM-IF input
FMIF1IN2	14	70 MHz FM-IF input
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output
FMIF2OUT2	20	FM mixer output
V_{REF}	21	reference voltage
AMIF2OUT1	22	AM mixer output
AMIF2OUT2	23	AM mixer output
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{PIF}	28	V_P IF amplifier

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM IF2 input 1
AMIF2IN2	34	AM IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjust
C_{AFC}	39	AFC capacitor
MPBUF	40	multipath buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjust
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjust
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
IAC_{IN}	46	IAC input
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
V_{MUTAML}	49	mute voltage / AM level
LEVELUNWEIG	50	level unweighted
$I_{ACCONTR}$	51	IAC control voltage
V_{PDIG}	52	V_P digital
SDA	53	SDA, pull-up to 5 V
SCL	54	SCL, pull-up to 5 V
BUSGND	55	bus ground
$V_{P8.5}$	56	V_P 8.5 V

In Car Entertainment (ICE) car radio TEA6822T

FEATURES

General

- FM mixer for conversion from FM-IF1 = 72.2 MHz to FM-IF2 = 10.7 MHz
- AM mixer for conversion from AM-IF1 = 10.7 MHz to AM-IF2 = 450 kHz
- FM-IF gain stage
- Crystal oscillator providing mixer frequencies and references for IF-count and stereo decoder
- FM quadrature demodulator with automatic centre frequency adjustment and THD compensation
- Level, multi-path and noise detectors
- Soft mute
- Stereo noise cancelling and variable de-emphasis
- PLL stereo decoder
- Noise blanker
- AM IF-amplifier and demodulator
- I²C-bus transceiver with interface to enable direct data transfer to radio front-end
- IF-count for AM and FM
- Reference frequency generation for PLL synthesizer.

Stereo decoder

- Adjustment-free PLL-VCO
- Pilot depending mono/stereo switching
- Analog control of mono/stereo blend
- Adjacent channel noise suppression (114 kHz)
- Pilot cancelled
- Analog control of de-emphasis
- Integrated low-pass filters for 190 kHz adjacent channel interferences and signal delay for interference absorption circuit.

GENERAL DESCRIPTION

The TEA6822T together with the TEA6810T/TEA6811T forms an AM/FM electronic tuned car radio in a double conversion receiver concept.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6822T	VSO56	plastic very small outline package; 56 leads	SOT190-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDA1}	analog supply current 1 (pin 5)	FM mode	18	21	25	mA
		AM mode	14	17	21	mA
$I_{19} + I_{20}$	total FM mixer output current		4.8	6.0	7.2	mA
$I_{22} + I_{23}$	total AM mixer output current		10	12	14	mA
V_{DDA2}	analog supply voltage 2 (pin 28)	note 1	7	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA2}	analog supply current 2 (pin 28)	FM mode	2.4	3.0	3.6	mA
V_{DDA3}	analog supply voltage 3 (+8.5 V; pin 56)	note 1	7	8.5	10	V
		operating range	8.1	8.5	8.9	V
I_{DDA3}	analog supply current 3 (pin 56)	FM mode	19	24	28	mA
		AM mode	9.5	12	15	mA
V_{DDD}	digital supply voltage 1 (+5 V; pin 5)	note 1	4.5	5.0	5.5	V
		operating range	4.75	5.0	5.25	V
I_{DDD}	digital supply current (pin 52)	note 1	8	10	12	mA
$\frac{S+N}{N}$	signal-plus-noise-to-noise ratio	ΔFM mode; f = 22.5 kHz at pins 43 and 47	66	75	–	dB
		AM mode; m = 0.3	54	60	–	dB
THD	total harmonic distortion	FM mode; Δf = 75 kHz	–	0.1	0.35	%
		AM mode	–	1.5	3	%
α_{cs}	channel separation (adjusted)		40	–	–	dB
T_{amb}	operating ambient temperature		−40	–	+85	°C

Note

1. IC is operating; specified parameters may deviate from limits which are valid for operating range.

BLOCK DIAGRAM

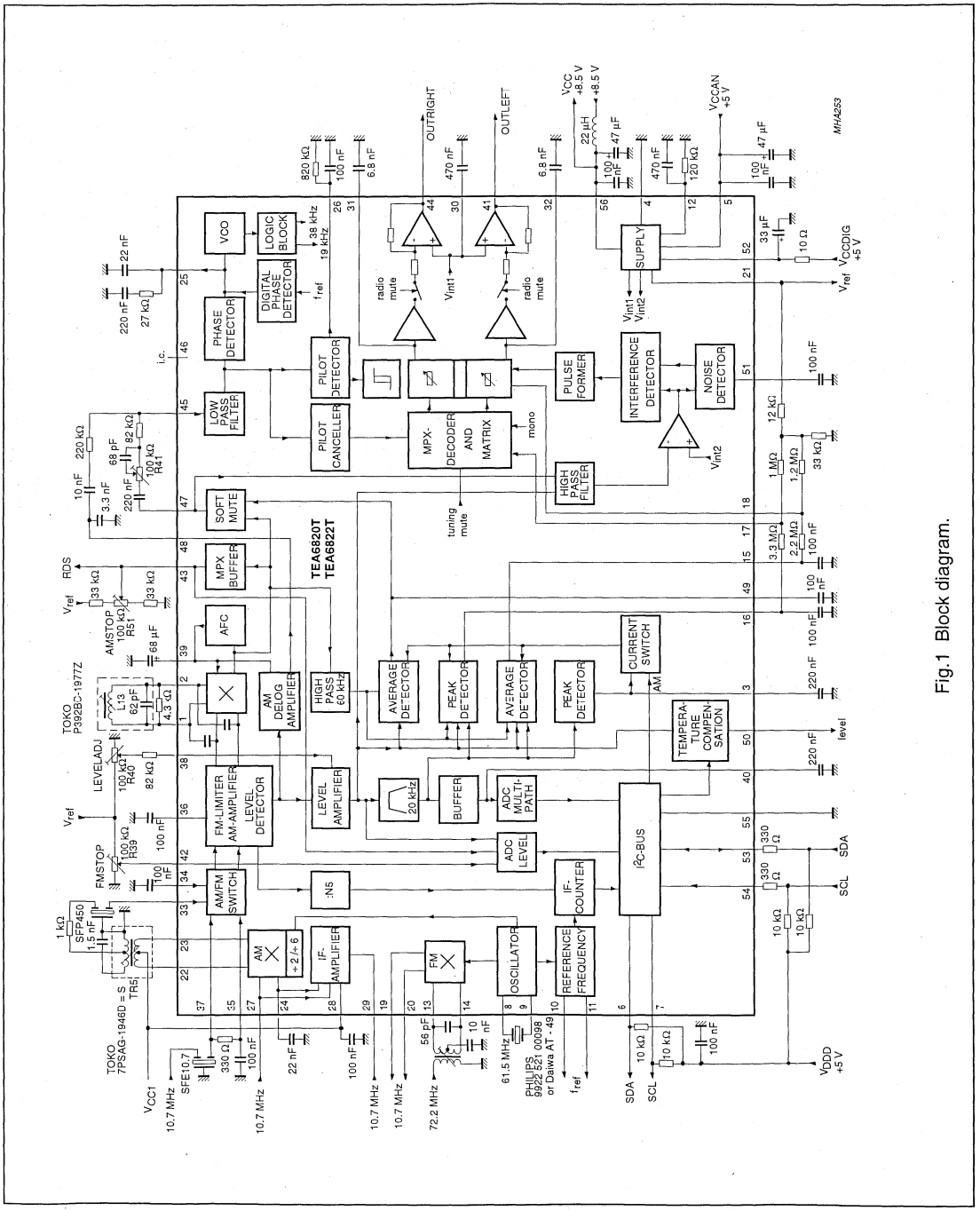


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
QDET1	1	demodulator tank 1
QDET2	2	demodulator tank 2
TSWITCH	3	time switch
AGND	4	analog ground
V_{DDA1}	5	analog supply voltage 1 (+5 V)
HFBUS1	6	HF bus 1; pull-up to 5 V
HFBUS2	7	HF bus 2; pull-up to 5 V
XTAL1	8	crystal oscillator 1
XTAL2	9	crystal oscillator 2
f_{ref1}	10	PLL reference output frequency 1
f_{ref2}	11	PLL reference output frequency 2
I_{ref}	12	reference current
FMIF1IN1	13	72 MHz FM-IF input 1
FMIF1IN2	14	72 MHz FM-IF input 2
TSDR	15	time constant for SDR
TSDS	16	time constant for SDS
V_{SDS}	17	SDS control voltage
V_{SDR}	18	SDR control voltage
FMIF2OUT1	19	FM mixer output 1
FMIF2OUT2	20	FM mixer output 2
V_{ref}	21	reference voltage
AMIF2OUT1	22	AM mixer output 1
AMIF2OUT2	23	AM mixer output 2
FMAMDEC	24	FM/AM 10.7 MHz decoupling
PHASEDET	25	phase detector
PILDET	26	pilot detector
FMAM10.7	27	FM/AM 10.7 MHz input
V_{DDA2}	28	analog supply voltage 2

SYMBOL	PIN	DESCRIPTION
FMIFAMPOUT	29	FM-IF amplifier output
AFGND	30	AF ground
DEEMPHR	31	de-emphasis capacitor right
DEEMPHL	32	de-emphasis capacitor left
AMIF2IN1	33	AM-IF2 input 1
AMIF2IN2	34	AM-IF2 input 2
FMIN2	35	FM limiter input
DCFEED	36	DC feed FM limiter
FMIN1	37	FM limiter input
LEVELADJ	38	level adjustment
C_{AFC}	39	AFC capacitor
MPBUF	40	multi-path buffer time constant
OUTLEFT	41	AF output left
FMSTOP	42	FMSTOP adjustment
RDS/AMSTOP	43	MPX for RDS/AMSTOP adjustment
OUTRIGHT	44	AF output right
MPXIN	45	stereo decoder MPX input
i.c.	46	internally connected
MPXOUT	47	FM demodulator MPX output
AMAFOUT	48	AM demodulator AF output
$V_{mute/AML}$	49	mute voltage/AM level
LEVELUNWEIG	50	level unweighted
IAC_{CONTR}	51	IAC control voltage
V_{DDD}	52	digital supply voltage
SDA	53	SDA; pull-up to 5 V
SCL	54	SCL; pull-up to 5 V
DGND	55	digital ground
V_{DDA3}	56	analog supply voltage 3 (8.5 V)

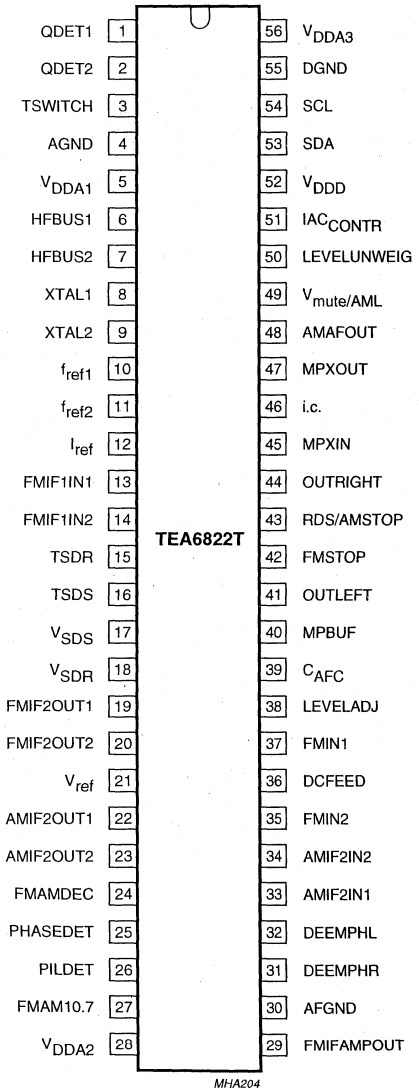


Fig.2 Pin configuration.

IF filter / amplifier / demodulator for FM radio receivers

TEA6850

FEATURES

- Improved dynamic selectivity and sensitivity because of tunable IF filter
- Fully integrated, frequency matched FM demodulator
- High linearity
- Unweighted level detector output
- Soft mute
- MPX output for RDS and diversity
- Internal source selector.

GENERAL DESCRIPTION

The TEA6850 is a monolithic bipolar integrated circuit for IF filtering, FM demodulation and level detection. Using IF filters tuned by the demodulated signal, dynamic selectivity and sensitivity are improved.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 7)	7	8.5	10	V
I_P	supply current (pin 7)	14	17.5	21	mA
DS200	dynamic selectivity for 200 kHz distance (EMF = 700 μV; filter bandwidth = 50 kHz)	22	27	–	dB
S/N	signal-to-noise ratio ($\Delta f = \pm 22.5$ kHz; f_m = 1 kHz)	61	67	–	dB
THD	total harmonic distortion ($\Delta f = \pm 75$ kHz; f_m = 1 kHz)	–	0.3	0.5	%
V_O	AF output signal at pin 4 (RMS value)	180	200	220	mV
T_{amb}	operating ambient temperature	−40	–	+85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TEA6850H	44	QFP	plastic	SOT307[1]

Note

1. SOT307-2; 1996 August 26.

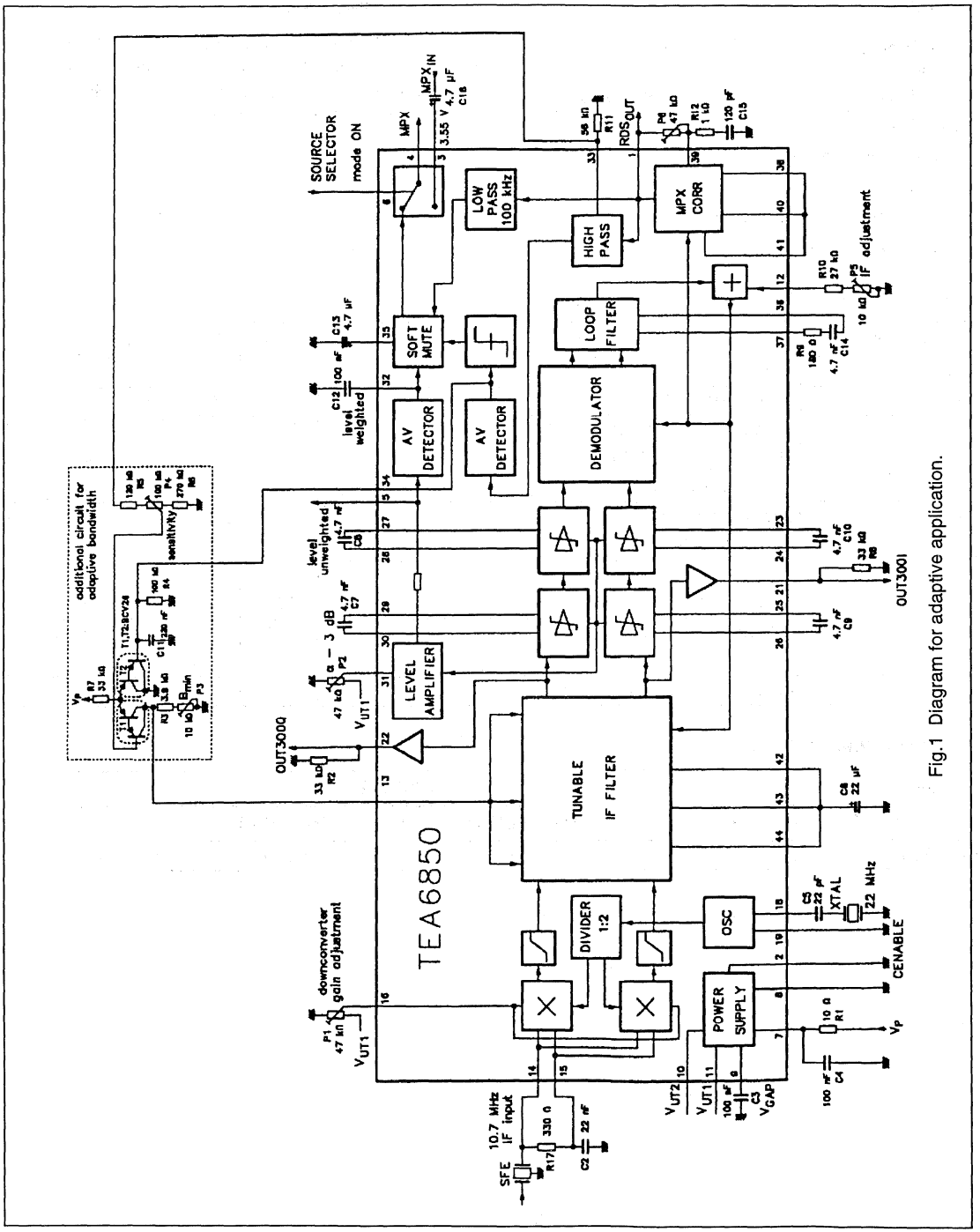
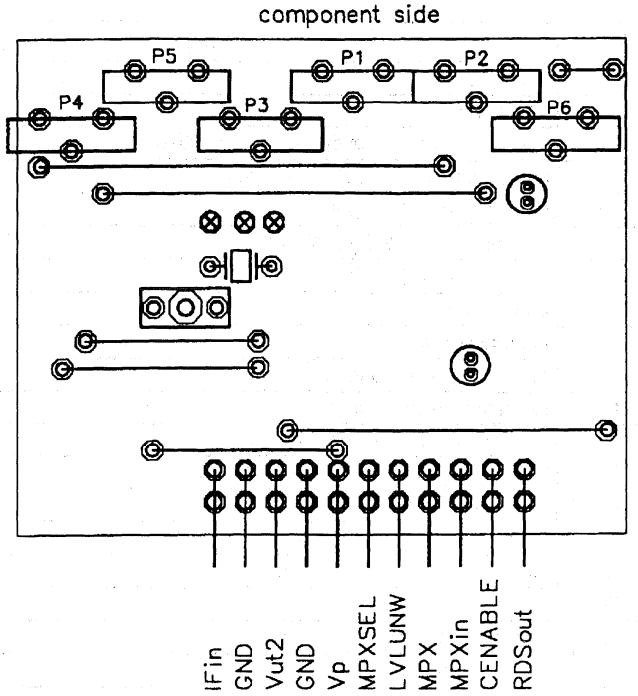


Fig.1 Diagram for adaptive application.



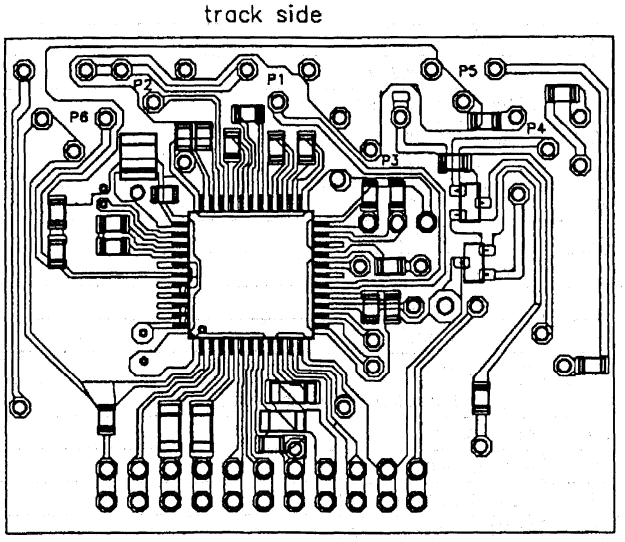


Fig.2 TEA6850H (adaptive version), printed- circuit board.

PINNING

SYMBOL	PIN	DESCRIPTION
RDS_{OUT}	1	output for RDS
CENABLE	2	chip enable
MPX_{IN}	3	external audio frequency input (MPX signal)
MPX	4	audio frequency output (MPX signal)
LVLUNW	5	unweighted level output
MPXSEL	6	source selector for MPX signal
V_P	7	supply voltage (8.5 V)
GND	8	ground (0 V)
V_{GAP}	9	internal reference voltage
V_{UT2}	10	reference voltage output
V_{UT1}	11	reference voltage output
IFADJ	12	input for IF filter frequency adjustment
BWADJ	13	input for IF filter bandwidth adjustment
IF_{IN}	14	IF signal input 1
IF_{INI}	15	IF signal input 2
GAINADJ	16	input for mixer gain adjustment
n.c.	17	not connected
CRYSTAL	18	crystal oscillator input
GND	19	oscillator ground
n.c.	20	not connected
OUT300I	21	IF filter output (0°)
OUT300Q	22	IF filter output (90°)
CLIM1I	23	IF limiter feedback 1
CLIM2I	24	IF limiter feedback 2
CLIM3I	25	IF limiter feedback 3
CLIM4I	26	IF limiter feedback 4
CLIM1Q	27	IF limiter feedback 5
CLIM2Q	28	IF limiter feedback 6
CLIM3Q	29	IF limiter feedback 7
CLIM4Q	30	IF limiter feedback 8
LVLADJ	31	input for level adjustment
LVLWEI	32	weighted level output
IHP60	33	input for high-pass –3 dB adjustment
CHPMUTE	34	output of rectified high-pass signal
CMUTE	35	mute input
DEMOLOOP1	36	demodulator output 1
DEMOLOOP2	37	demodulator output 2
COP2	38	MPX correction output 2
CON2	39	MPX correction input 2
COO1	40	MPX correction output 1

Fast radio tuning PLL frequency synthesizer

TSA6060

FEATURES

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high-performance one-input-two-output, tuning voltage amplifier for the AM and FM loop filters
- On-chip two-level current amplifier (charge pump) for loop gain adjustment
- One reference oscillator (4 or 8 MHz) for both AM and FM
- High-speed tuning provided by a powerful digital memory phase detector
- 40 kHz output reference frequency for communication between the FM/IF system and microcontroller-based tuning interface IC (TEA6100)
- Oscillator frequency range of 500 kHz to 30 MHz and 30 MHz to 200 MHz
- Four selectable reference frequencies: 1, 10, 25 or 50 kHz, for both tuning ranges
- I²C-bus interface to a microcontroller
- Software controlled band switch output
- In-lock detector output.

APPLICATIONS

- FM mains and car radios
- VHF receivers 30 to 200 MHz.

GENERAL DESCRIPTION

The TSA6060 is a frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). The device performs all the tuning functions of a PLL radio tuning system.

The IC is designed for application in all types of radio receivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC1}	supply voltage (pin 3)		4.5	5.0	5.5	V
V_{CC2}	supply voltage (pin 16)		V_{CC1} + 1	8.5	12.0	V
I_{CC1}	supply current (pin 3)	no outputs loaded	–	15	–	mA
I_{CC2}	supply current (pin 16)	no outputs loaded	0.7	1.0	1.5	mA
f_{iAMmax}	maximum AM input frequency		30	–	–	MHz
f_{iAMmin}	minimum AM input frequency		–	–	500	kHz
f_{iFMmax}	maximum FM input frequency		200	–	–	MHz
f_{iFMmin}	minimum FM input frequency		–	–	30	MHz
$V_{iAM(rms)}$	AM input voltage (RMS value)	V_{iFM} = 0 V; f_i < 15 MHz	30	–	500	mV
$V_{iFM(rms)}$	FM input voltage (RMS value)	V_{iAM} = 0 V	20	–	300	mV
P_{tot}	total power dissipation		–	100	–	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA6060	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TSA6060T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

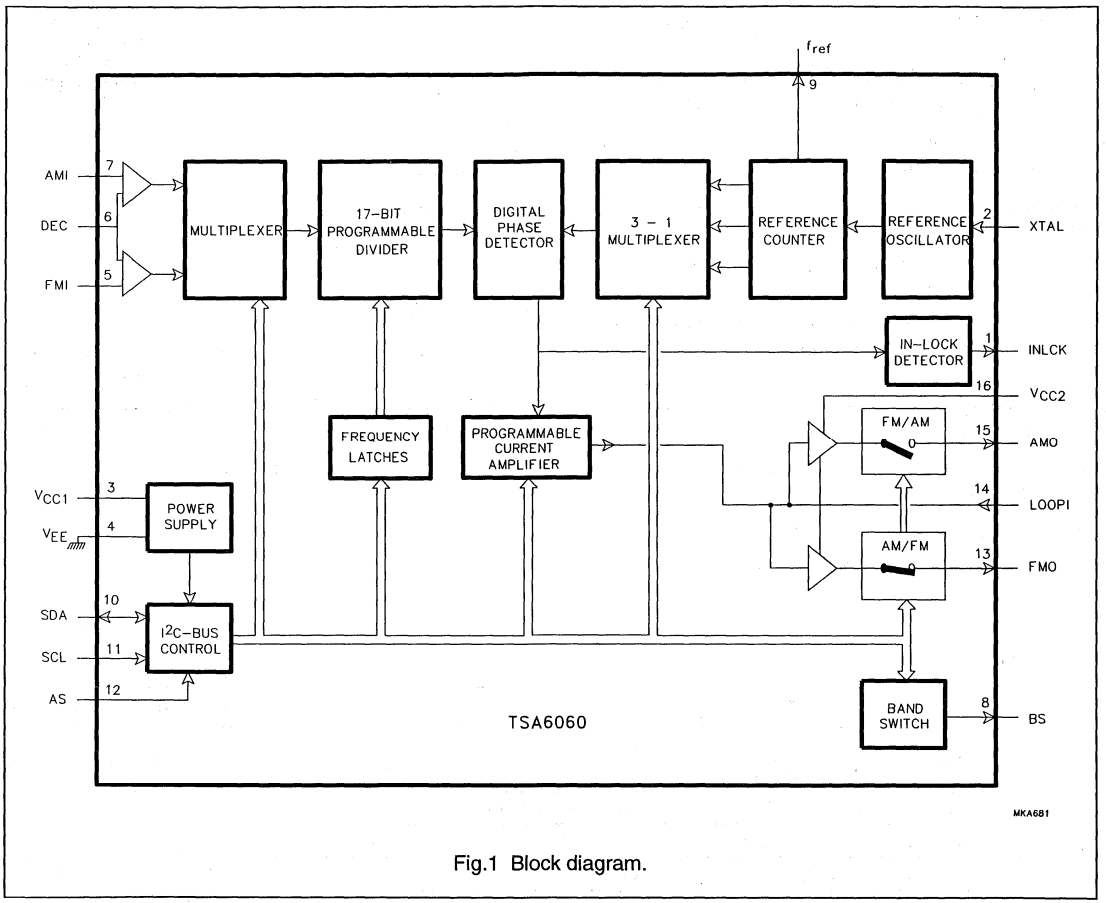


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INCLK	1	in-lock detector output
XTAL	2	crystal reference oscillator input
V_{CC1}	3	supply voltage (PLL supply 1)
V_{EE}	4	ground
FM_I	5	FM VCO input
DEC	6	prescaler decoupling
AM_I	7	AM VCO input
BS	8	band switch output
f_{ref}	9	40 kHz reference output
SDA	10	serial data input (I^2C-bus)
SCL	11	serial clock input (I^2C-bus)
AS	12	address select input (I^2C-bus)
FM_O	13	FM output for external loop filter
$LOOP_I$	14	tuning voltage amplifier input
AM_O	15	AM output for external loop filter
V_{CC2}	16	supply voltage (PLL supply 2)

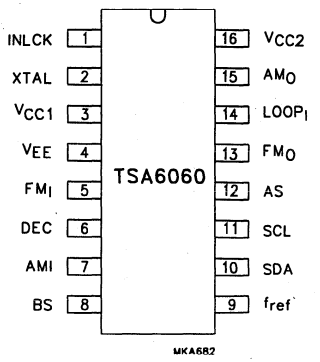


Fig.2 Pin configuration.

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DATA HANDBOOK SYSTEM

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IC15	FAST TTL Logic Series
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IC20	80C51-based 8-bit Microcontrollers
IC22	Desktop Video
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MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

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